PHY 359 2.0 / ASP 487 2.0 Telecommunication

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Digital Modulation

(FSK – Frequency Shift Keying)

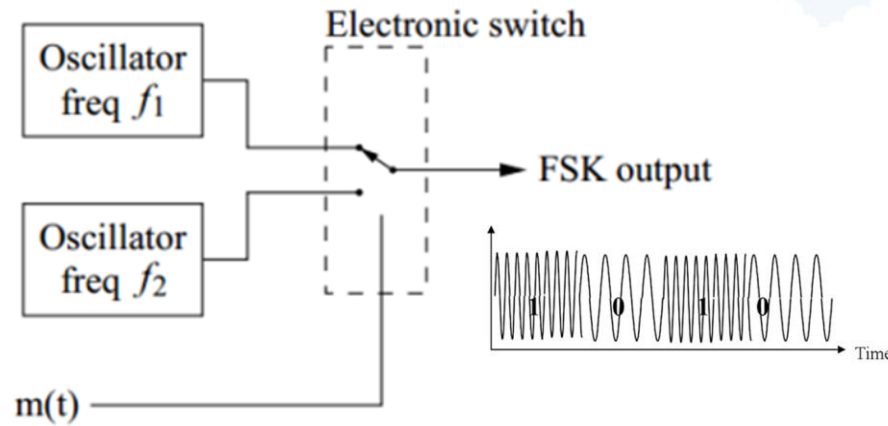
Frequency shift keying (FSK)

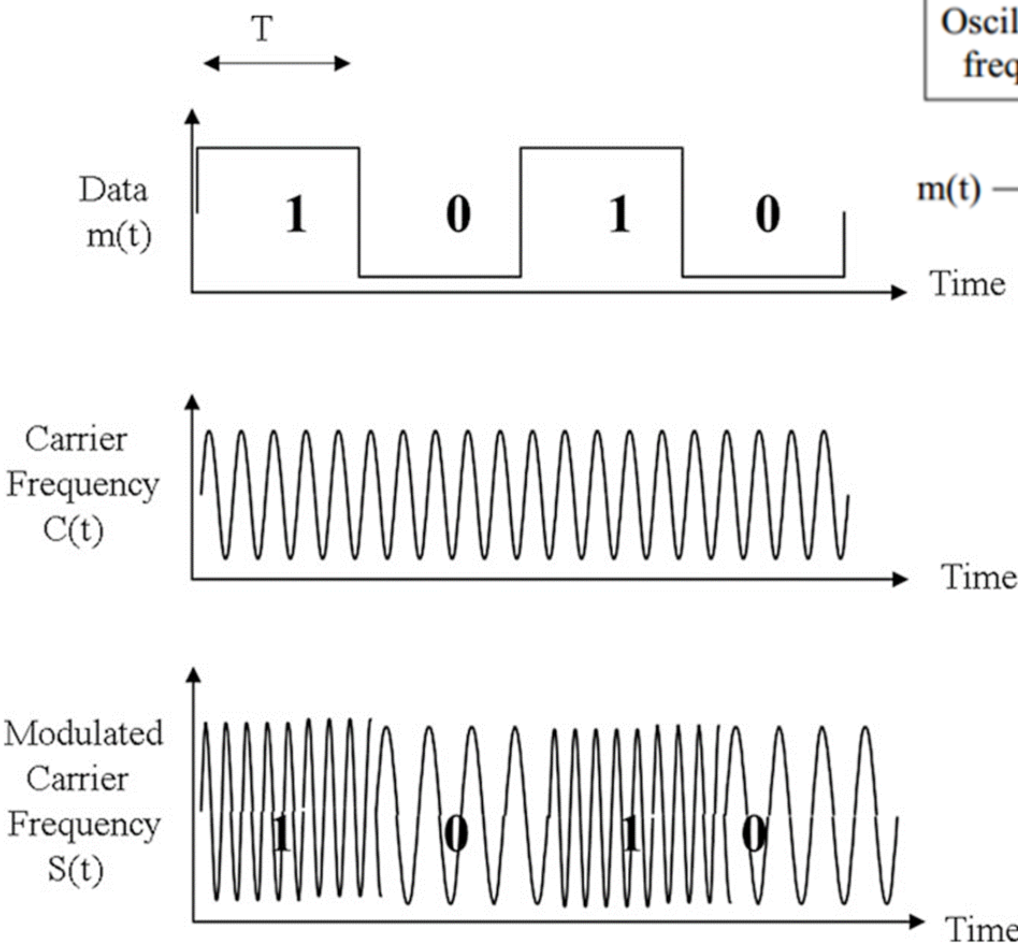
- FSK is a method of digital modulation that utilizes frequency shifting of the relative frequency content of the signal. The signal is to be modulated and transmitted in binary; this is referred to as binary FSK (BFSK).
- Where the carrier frequency changes in discrete levels, in accordance with the input signal:

Binary 0 (bit 0): Frequency = $f + \Delta f$
Binary 1 (bit 1): Frequency = $f - \Delta f$

- Output is the FSK-modulated carrier, which has two frequencies f_1 and f_2, corresponding to the binary input signal
- These frequencies correspond to the messages binary 0 and 1, respectively.

Frequency shift keying (FSK)





m(t) - Input modulating digital signal
C(t) - Carrier signal
S(t) - ASK modulated signal

FSK – Modulation Technique

- This is an indispensable task in digital communications, where redundant bits are added to the raw data, enabling the receiver to detect and correct bit errors during transmission.
- Many error-coding schemes are available, and a simple coding technique, known as "Block Coding" illustrates the concept.
- Encoded ASK modulation scheme using (15, 8) block code where an 8-bit data block is formed as M-rows and N-columns (M = 4, N = 2).
- The product MN = k = 8 is the dimension of the information bits before coding.

Used Even parity

Data set – 8 bit

0	0	0	1	1	0	1	1

			P_H
	0	0	**0**
	0	1	**1**
	1	0	**1**
	1	1	**0**
P_V	**0**	**0**	**0**

P_H - Horizontal parity
P_V - Vertical parity

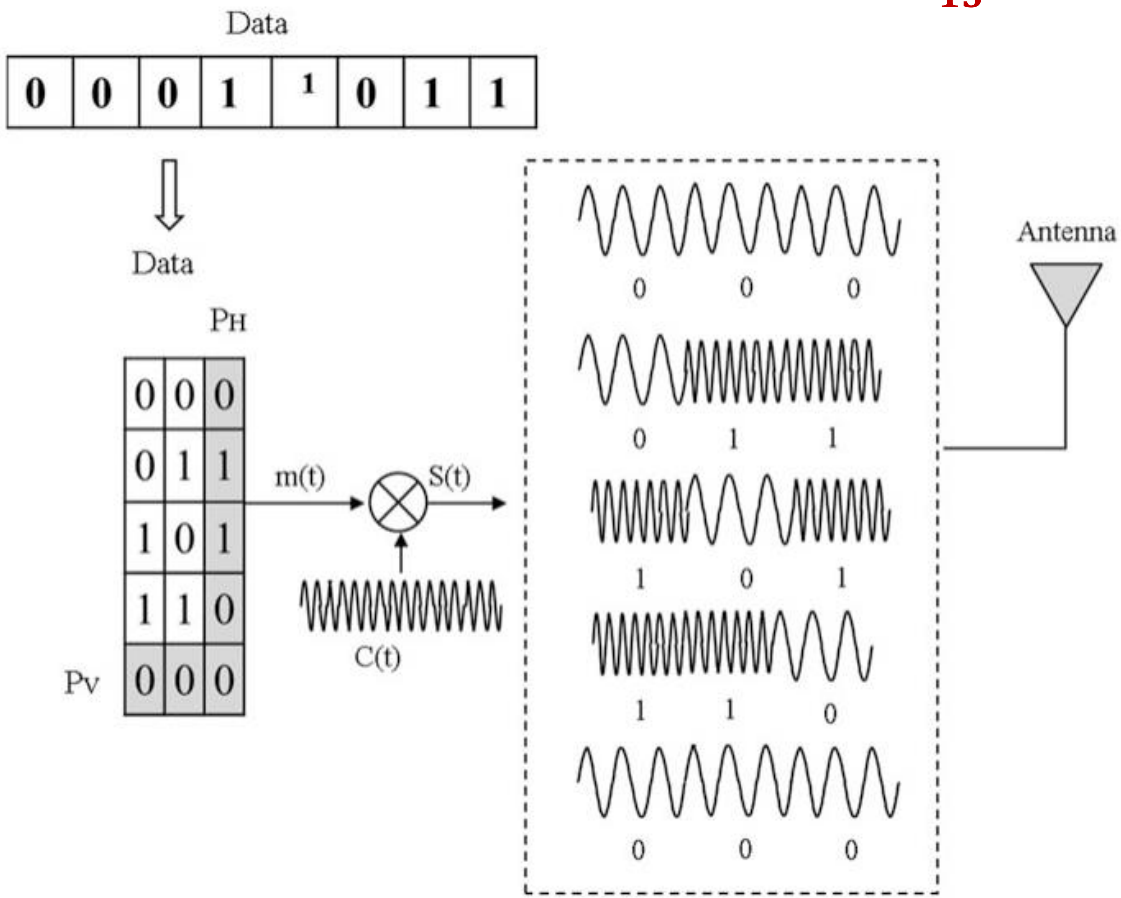
- ASK modulated and transmitted row by row.
- The resulting augmented dimension is given by the product (M + 1) (N + 1) = n = 15

FSK – Modulation Technique

- **Code Rate:** $r = \frac{MN}{(M+1)(N+1)} = \frac{4\times 2}{(4+1)(2+1)} = \frac{8}{15}$

- If the coded bit rate is $\mathbf{R_{bcoded}}$ and the Uncoded bit Rate is $\mathbf{R_{buncoded}}$

$$R_{bcoded} = \frac{Uncoded\ Bit\ Rate}{Code\ Rate} = \frac{R_{buncoded}}{r} = \frac{R_{buncoded}}{\frac{8}{15}} = \frac{R_{buncoded}\times 15}{8}$$



FSK – Modulation Technique

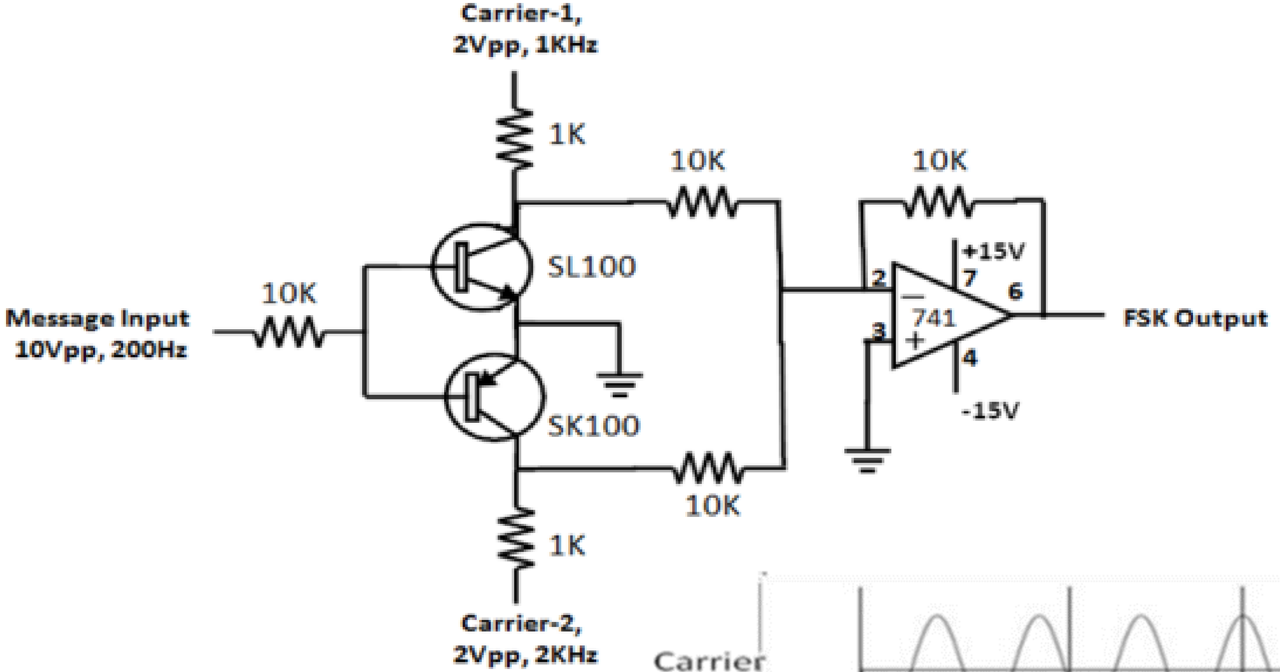
$$\begin{aligned}
&\text{Input Data:} && m(t) = 0 \text{ or } 1 \\
&\text{Carrier Frequency:} && C(t) = A\cos(\omega t) \\
&\text{Modulated Carrier:} && S(t) = A\cos(\omega - \Delta\omega)t, \text{For } m(t) = 1 \\
& && S(t) = A\cos(\omega + \Delta\omega)t, \text{For } m(t) = 0
\end{aligned}$$

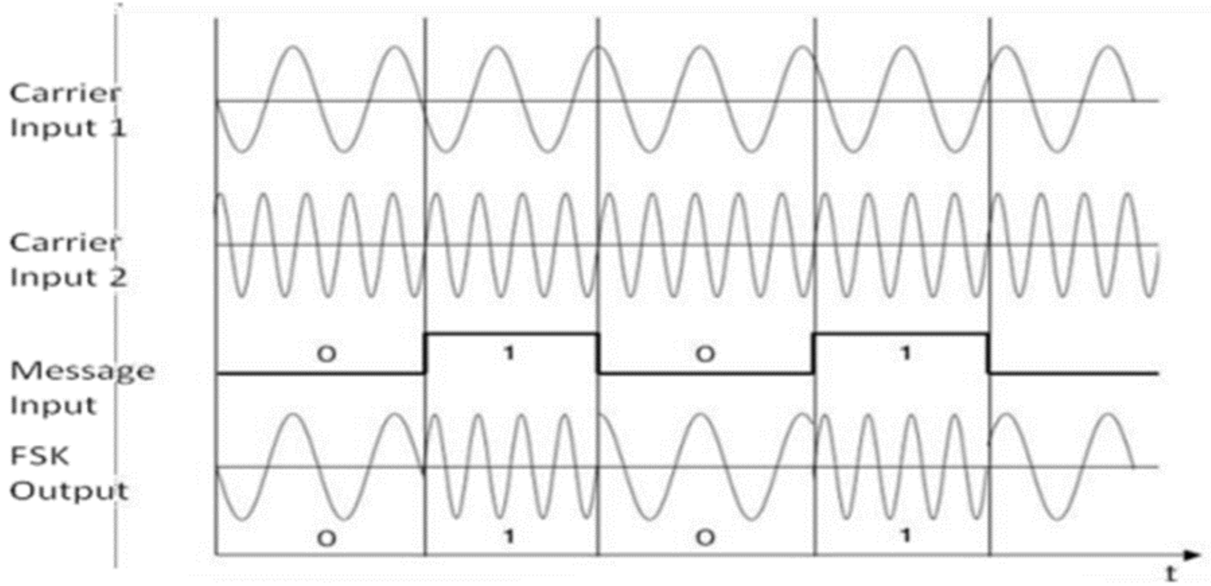
$$\begin{aligned}
A &= \text{Frequency of the carrier} \\
\omega &= \text{Nominal frequency of the carrier frequency} \\
\Delta\omega &= \text{Frequency deviation.}
\end{aligned}$$

- The input digital signal is the encoded bit sequence we want to transmit.
- Carrier is the radio frequency without modulation.
- Output is the FSK-modulated carrier, which has two frequencies corresponding to the binary input signal.
- For binary signal 1, the carrier changes to $f_c - \Delta f$.
- For binary signal 0, the carrier changes to $f_c + \Delta f$.
- The total frequency deviation is $2\Delta f$.

Basic FSK – Modulator Circuit

FSK – Modulator using Transistor and OP-Amp





FSK Demodulation

- For FSK, the receiver needs to utilize two band-pass filters tuned to the appropriate carrier frequency.

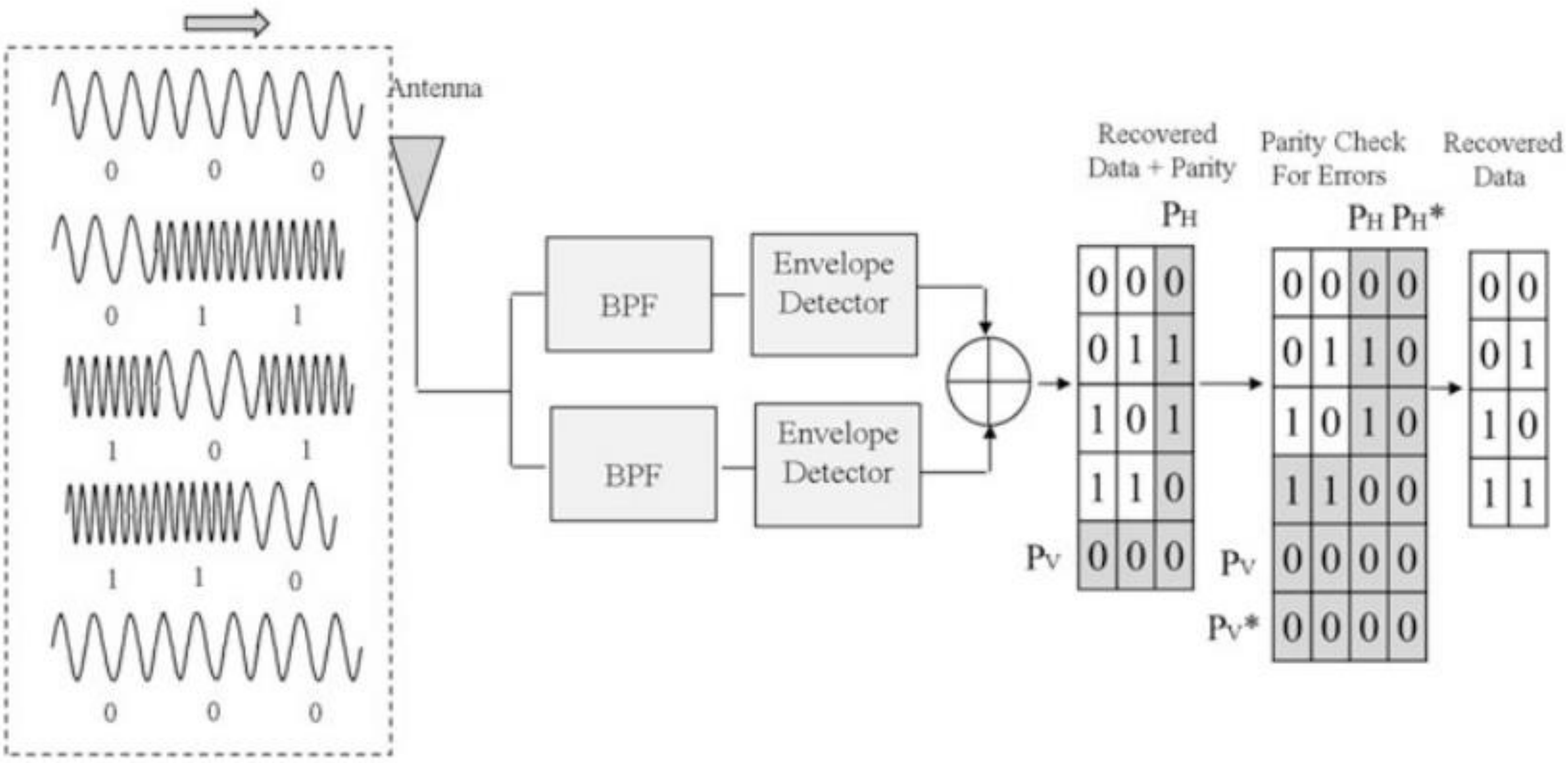
- Since the nominal carrier frequency and the frequency deviation are known, this is relatively straightforward. One band-pass filter will be centered at the frequency f_1 and the other at f_1.

- When the signal enters the receiver, it passes through the respective filter, and the corresponding bit value is made. Then, the receiver determines the value of each bit to recover the encoded data block, including horizontal and vertical parities.

- To ensure that the bits are decoded correctly, the frequency deviation needs to be chosen with the limitations of the filters in mind to eliminate crossover.

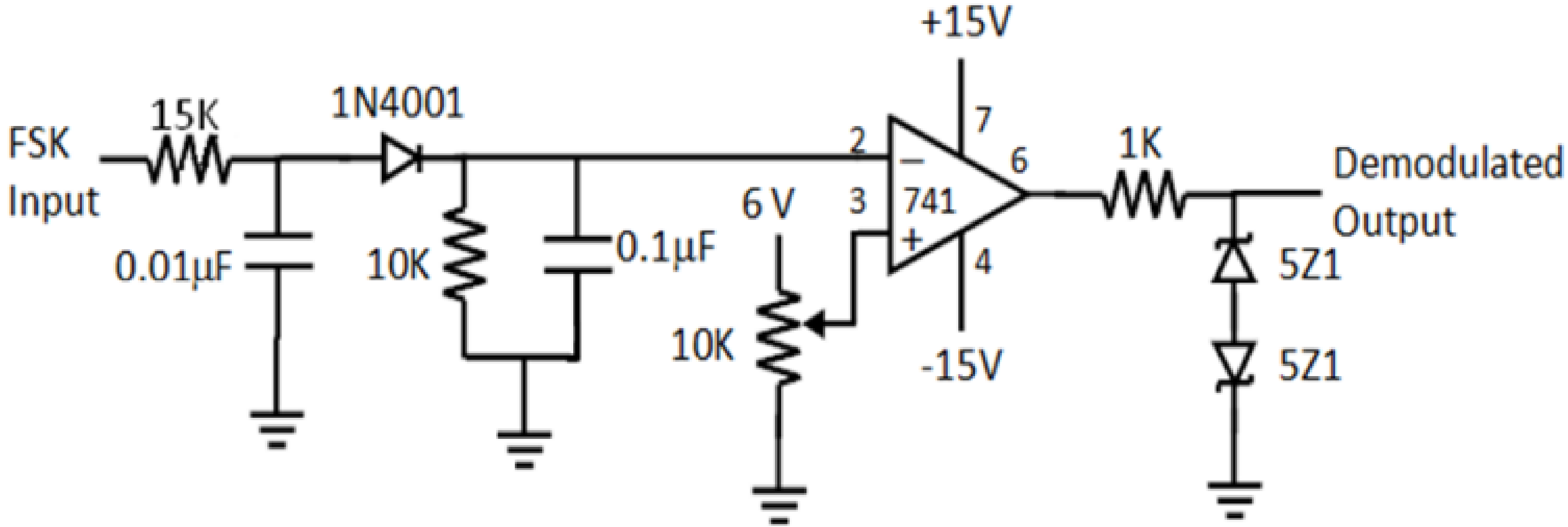
FSK Demodulation

- Then, the receiver appends horizontal and vertical parities (P_H* and P_V*) to check for errors and recover the data block.
- If there is an error, there will be a parity failure in P_H* and P_V* to pinpoint the error.



FSK Demodulation

Basic Demodulation Circuit



FSK Bandwidth

In digital communications, data is generally referred to as a non-periodic digital signal. It has two values:

- Binary-1 = High, Period = T
- Binary-0 = Low, Period = T

Also, data can be represented in two ways:

- Time domain representation and
- Frequency domain representation

The time domain representation, known as non-return-to-zero (NRZ), is given by:

$$\begin{aligned} V(t) &= V \qquad &< 0 < t < T \\ &= 0 \qquad &\text{elsewhere} \end{aligned}$$

FSK Bandwidth

The frequency domain representation is given by “Fourier transform”

$$V(\omega) = \int_0^T V \cdot e^{-j\omega t} dt$$

$$|V(\omega)| = VT\left[\frac{\sin(\omega T/2)}{\omega T/2}\right]$$

P(ω) - Power spectral density

$$P(\omega) = \left(\frac{1}{T}\right)|V(\omega)|^2 = V^2 T\left[\frac{\sin(\omega T/2)}{\omega T/2}\right]^2$$

- The bandwidth of the power spectrum is proportional to the frequency.
- The one-sided bandwidth is given by the ratio $f/f_b = 1$. So, the one-sided bandwidth = $f = f_b$, where $f_b = R_b = 1/T$, T being the bit duration. The general equation for two-sided response is given by:

$$V(\omega) = \int_{-\infty}^{\infty} V(t) \cdot e^{-j\omega t} dt$$

FSK Bandwidth

- V(ω) - two-sided spectrum of V(t).
- This is due to both positive and negative frequencies used in the integral.
- The function can be a voltage or a current.

$$V(\omega) = \int_{-\propto}^{\propto} V(t) \cdot e^{-j\omega t} dt$$

Two-sided bandwidth (BW) = $2R_b$ (R_b - Bit rate before coding)

FSK Bandwidth

Fig (a): Discrete-time digital signal

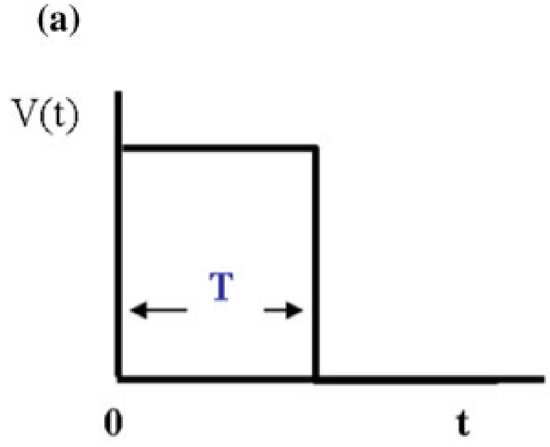


Fig (b): one-sided power spectral density

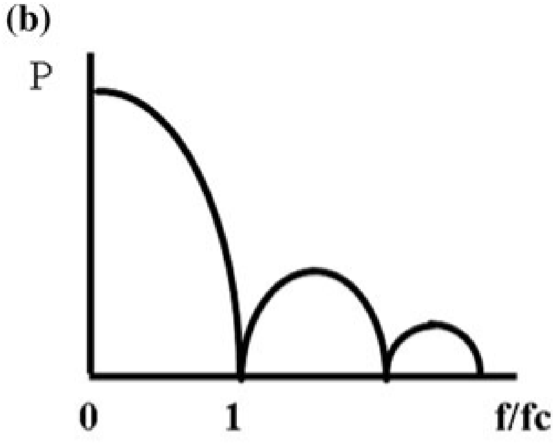
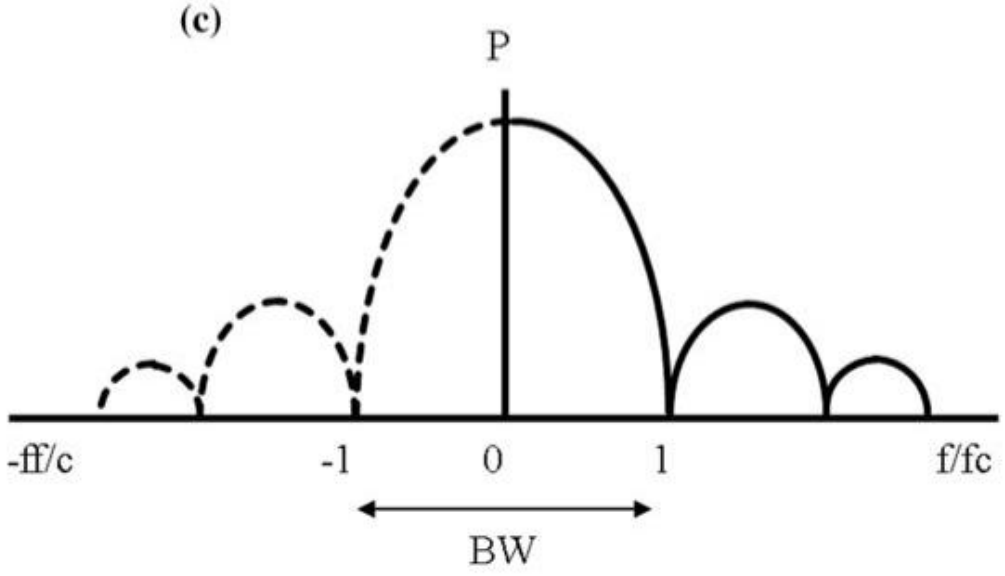


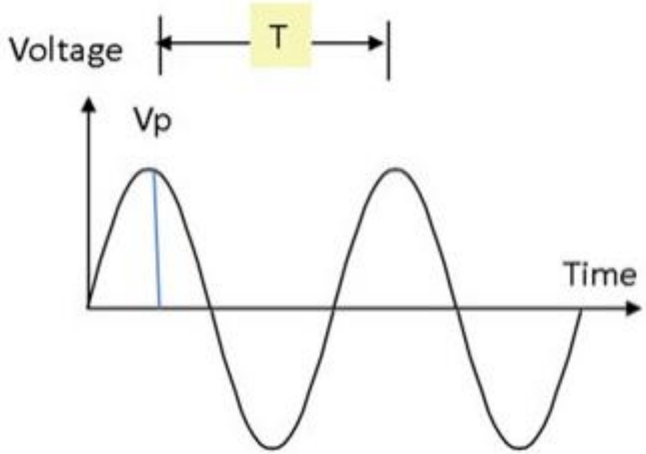
Fig (c): Two-sided power spectral density

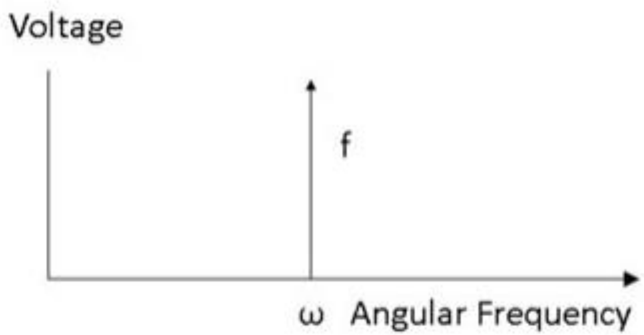


FSK Bandwidth

$V(t) = V_p \sin(\omega t_c)$ V_P = Peak voltage

$\omega_c = 2\pi f_c$
f_c = Carrier frequency in Hz





Input Data: $m(t) = 0 \text{ or } 1$
Carrier Frequency: $C(t) = A\cos(\omega t)$
Modulated Carrier: $S(t) = A\cos(\omega - \Delta\omega)t$, For $m(t) = 1$
$S(t) = A\cos(\omega + \Delta\omega)t$, For $m(t) = 0$

$S(t)$ = The modulated carrier
A = Amplitude of the carrier
ω = Nominal frequency of the carrier
$\Delta\omega$ = Frequency deviation

FSK Bandwidth

Notice: The carrier frequency after FSK modulation varies back and forth from the nominal frequency f_c by $\pm \Delta f_c$, where Δf_c is the frequency deviation. The FSK bandwidth is given by:

$$\begin{aligned} \mathrm{BW} &= 2(f_b + \Delta f_c) \\ &= 2f_b(1 + \Delta f_c / f_b) \\ &= 2f_b(1 + \beta) \end{aligned}$$

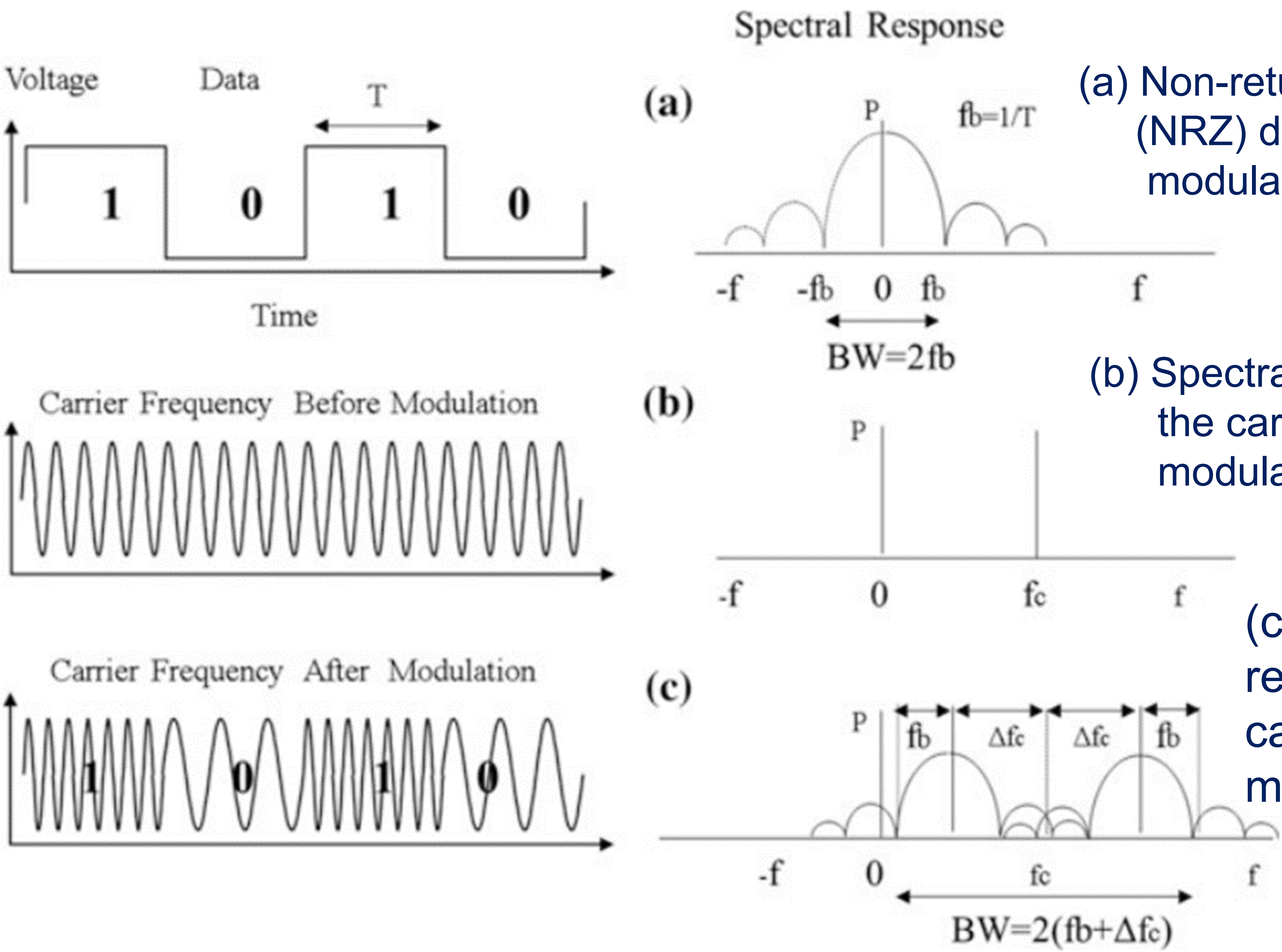
"Carson's rule"

$\beta = \Delta f_c / f_b$ (modulation index)

f_b - Coded bit frequency (bit rate R_b)

FSK Bandwidth

The spectral response



(a) Non-return-to-zero (NRZ) data before modulation.

(b) Spectral response of the carrier before modulation.

(c) The Spectral response of the carrier after modulation.

FSK Bandwidth

Example:

Consider the Bit rate before coding: R_{b1} = 10 kb/s and Code rate: r = 8/15 and the modulation index (β) = 1 for the FSK modulation. Find:

(1) The bit rate after coding: R_{b2} (Ans: 18.75 kb/s)

(2) Transmission bandwidth: BW (Ans: 75 kHz)

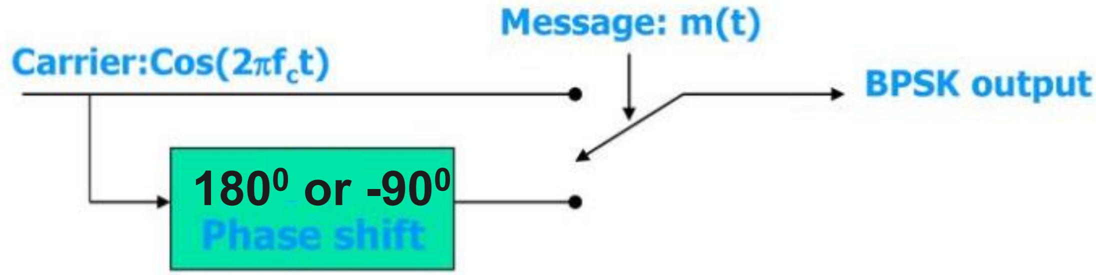
Phase shift keying (PSK)

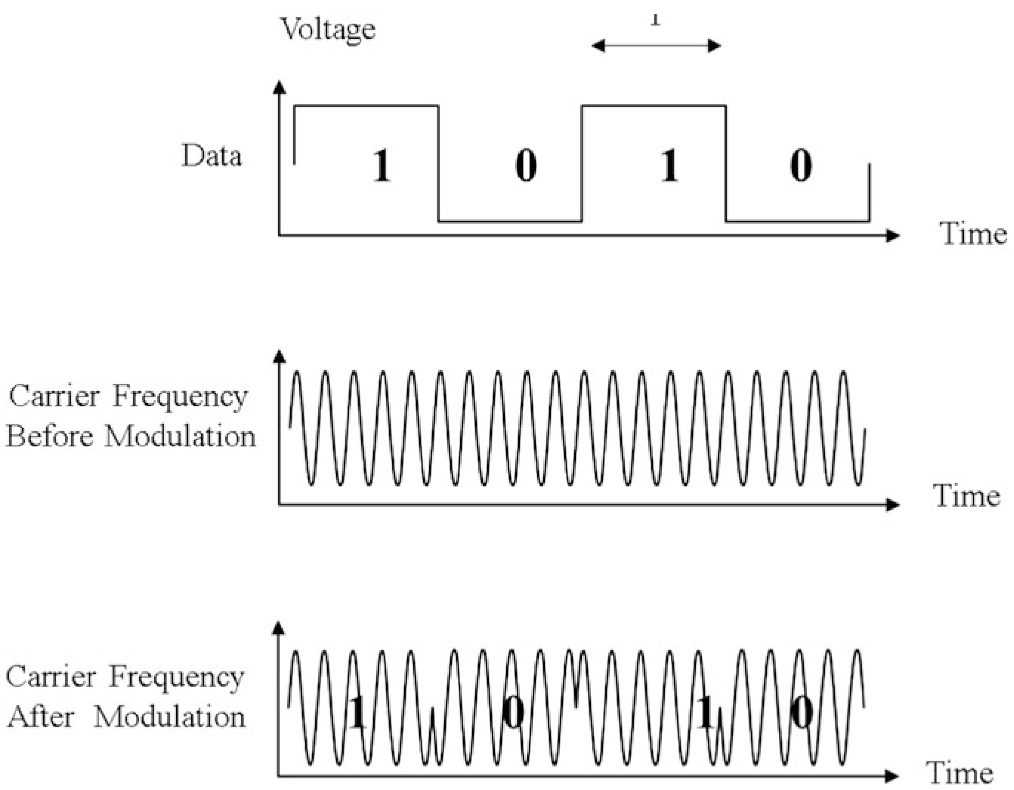
- Binary Phase Shift Keying (BPSK) Modulation
- QPSK Modulation
- 8PSK Modulation
- 16PSK Modulation

Binary Phase Shift Keying (BPSK)

- PSK is a method of digital modulation that utilizes the phase of the carrier to represent the digital signal. The signal to be modulated and transmitted is binary; this is referred to as binary PSK (BPSK).
- Where the phase of the carrier changes in discrete levels, in accordance with the input signal:
  Binary 0 (bit 0): Phase1 = 0°
  Binary 1 (bit 1): Phase2 = 180°
- Output is the BPSK-modulated carrier, which has two phases ϕ_1 and ϕ_2 corresponding to the two information bits.

Binary Phase shift keying (BPSK)





Binary Phase shift keying (BPSK)

Binary Phase Shift Keying (BPSK) Modulation

- Phase shift keying (PSK) is a method of digital modulation that utilizes phase shifting of the relative phase content of the signal.
- The signal to be modulated and transmitted is binary, which is encoded before modulation.
- This is an indispensable task in digital communications, where redundant bits are added to the raw data that enable the receiver to detect and correct bit errors if they occur during transmission.

BPSK – Modulation Technique

- Many error-coding schemes are available, and a simple coding technique, known as “Block Coding” illustrates the concept.
- Encoded ASK modulation scheme using (15, 8) block code where an 8-bit data block is formed as M-rows and N-columns (M = 4, N = 2).
- The product MN = k = 8 is the dimension of the information bits before coding.

Data set – 8 bit

0	0	0	1	1	0	1	1

P_H - Horizontal parity
P_V - Vertical parity

Used Even parity

			P_H
	0	0	**0**
	0	1	**1**
	1	0	**1**
	1	1	**0**
P_V	**0**	**0**	**0**

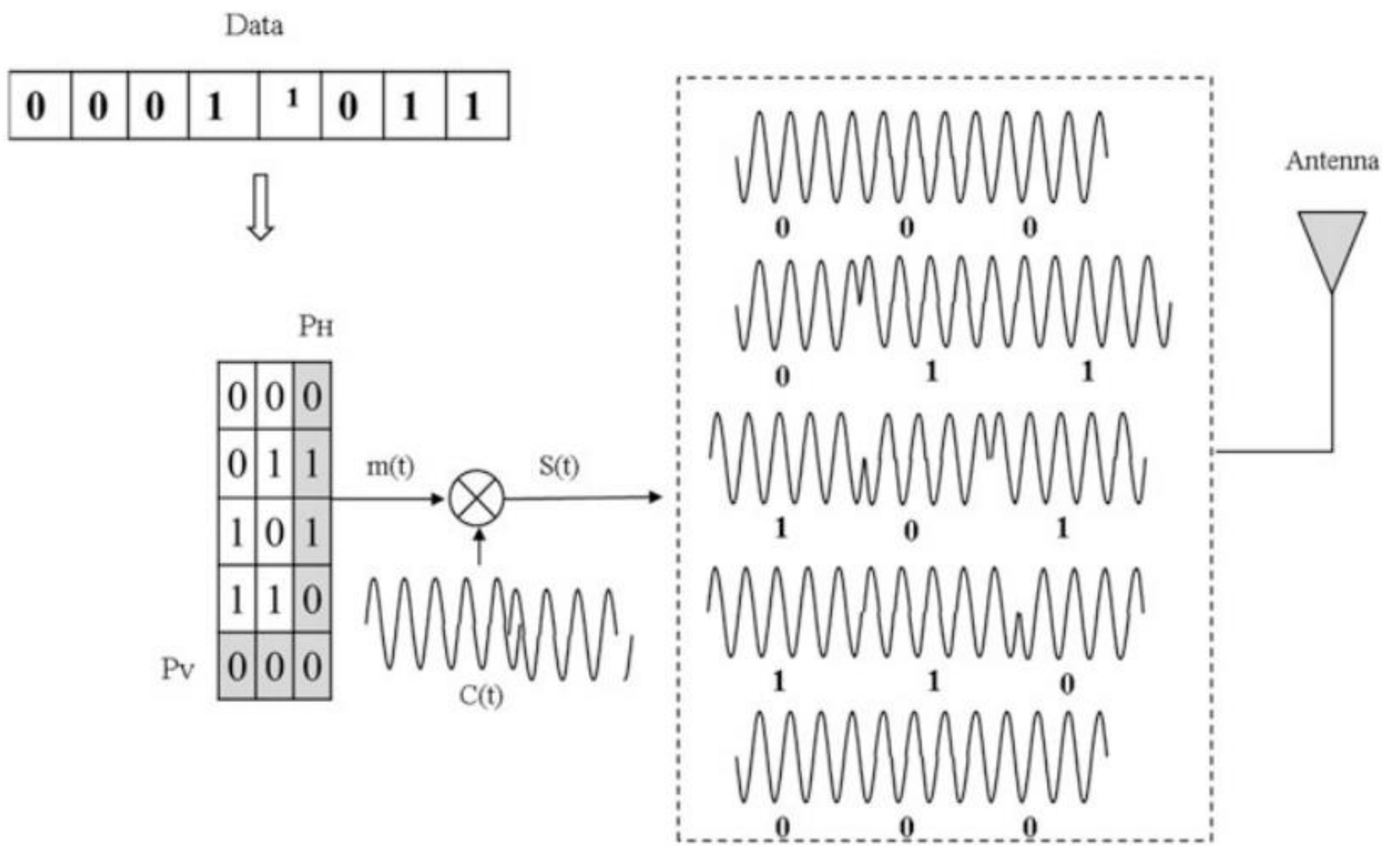
- ASK modulated and transmitted row by row.
- The resulting augmented dimension is given by the product (M + 1) (N + 1) = n = 15

BPSK – Modulation Technique

- **Code Rate:** $r = \frac{MN}{(M+1)(N+1)} = \frac{4\times 2}{(4+1)(2+1)} = \frac{8}{15}$

- If the coded bit rate is $\mathbf{R_{bcoded}}$ and the Uncoded bit Rate is $\mathbf{R_{buncoded}}$

$$R_{bcoded} = \frac{Uncoded\ Bit\ Rate}{Code\ Rate} = \frac{R_{buncoded}}{r} = \frac{R_{buncoded}}{\frac{8}{15}} = \frac{R_{buncoded}\times 15}{8}$$



BPSK – Modulation Technique

Input Data : $m(t) = 0 \text{ or } 1$

Carrier Frequency : $C(t) = A\cos(\omega_{ct})$

Modulated Carrier : $S(t) = A_c \cos[\omega_c t + 2\pi/M)m(t)]$ $m(t) = 0, 1, 2, 3, \ldots M - 1$

A_c = Amplitude of the carrier frequency

ω_c = Angular frequency of the carrier

$M = 2, 4, 8, 16, \ldots$

In BPSK, there are two phases 1 bit/phase$(M = 2)$

In QPSK, there are four phases, 2-bits/phase, $M = 4$

In 8PSK, there are 8 phases, 3-bits/phase, $M = 8$

In 16PSK, there are 16 phases, 4-bits/phase, $M = 16$

- The Input digital signal is the encoded bit sequence we want to transmit;
- Carrier is the radio frequency without modulation;
- Output is the PSK-modulated carrier, which has two phases corresponding to the binary input signals;
- For binary signal 0, $\varphi = 0°$; and
- For binary signal 1, $\varphi = 180°$.

BPSK – Modulation Technique

- The BPSK modulator can also be represented as a signal constellation diagram with **M = 2**, **1** bit per phase.

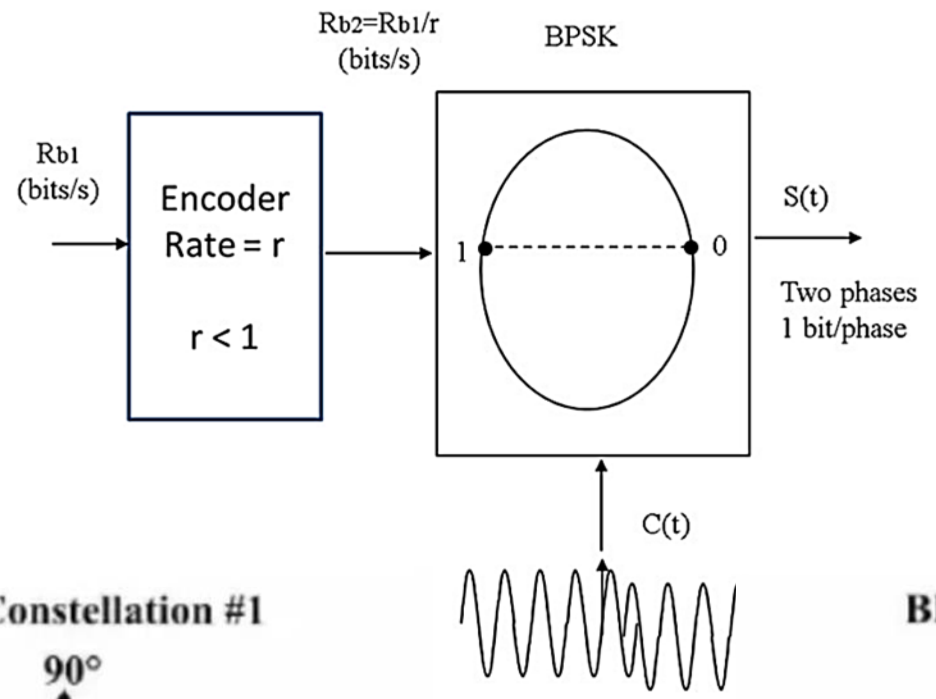
- This is shown in the figure, where the input raw data, having a bit rate R_{b1}, is encoded using a rate **r** encoder.

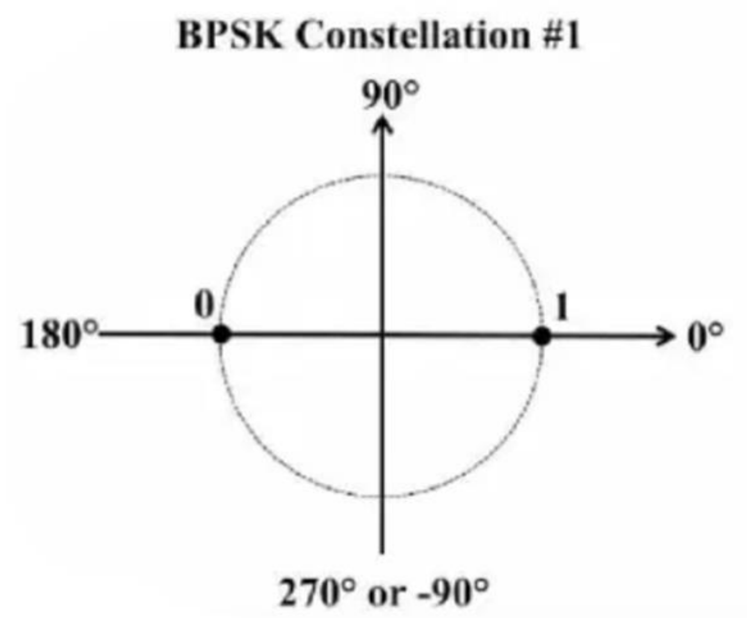
- The encoded data, having a bit rate R_{b2}, = R_{b1}/r ($r < 1$), is modulated by the BPSK modulator as shown in the figure.

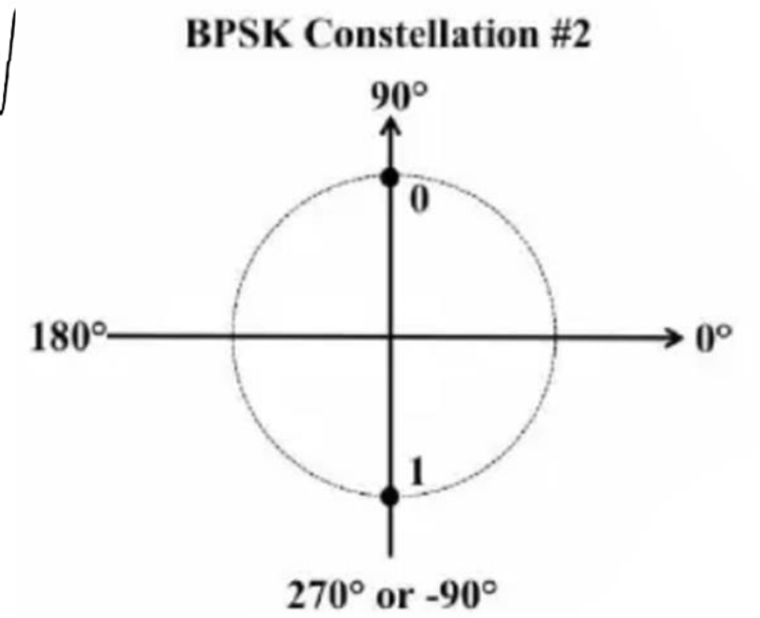
- The BPSK modulator takes one bit at a time to construct the phase constellation having two phases, also known as "Symbols," where each symbol represents one bit. The symbol rate is therefore the same as the encoded bit rate R_{b2}.

- BPSK modulator specifications: 2 phases or 2 symbols; 1-bit/symbol, These specifications govern the transmission bandwidth.

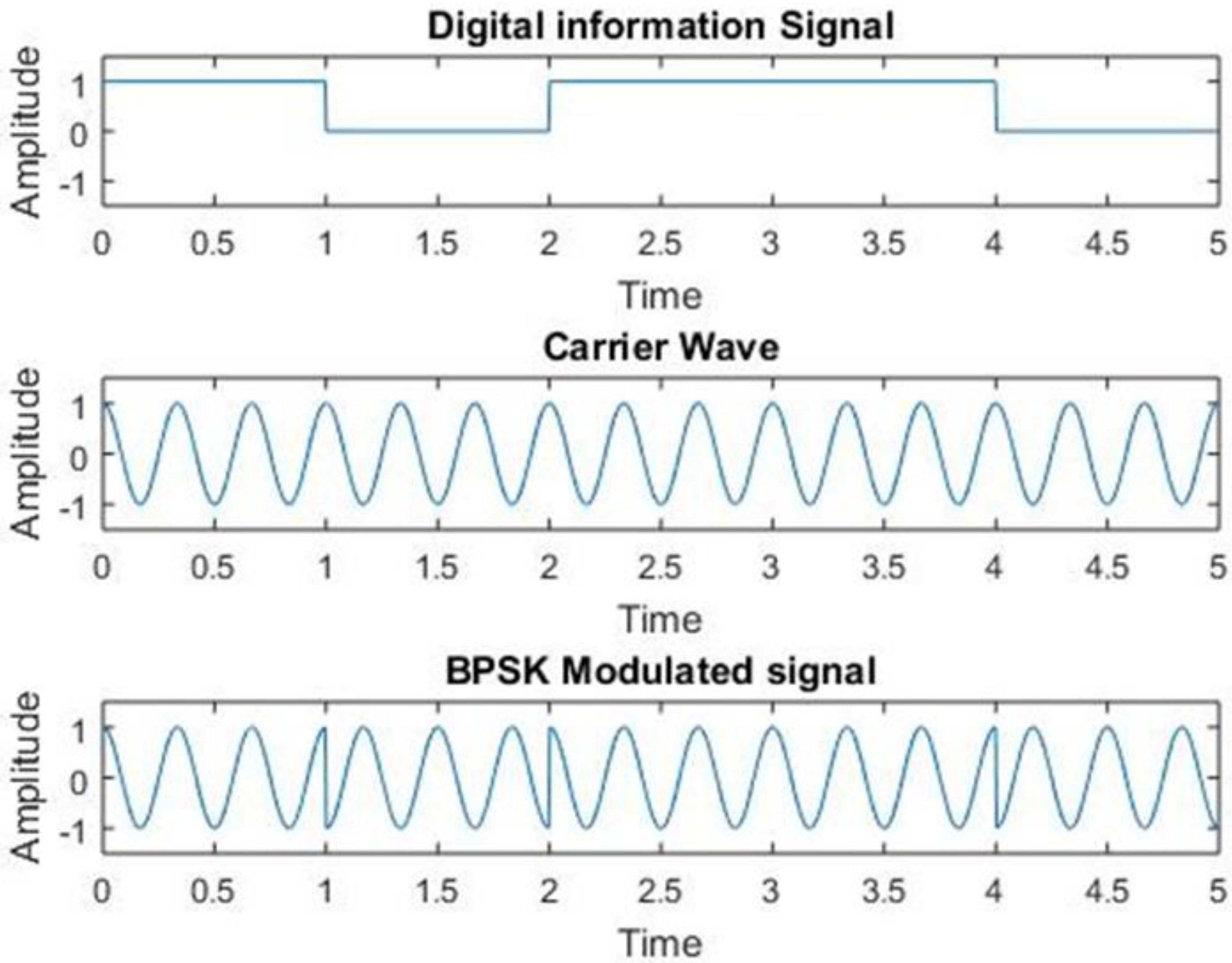
BPSK – Modulation Technique







BPSK – Modulation Technique



BPSK – Modulation Technique

- BPSK uses two phases which are separated by 180° (ex: 0 and π phase) and encodes one bit per symbol.
- Phases are not exactly pointed because the modulated signal takes some noise level or distortion, and it makes the incorrect decision by the demodulation techniques.
- BPSK The general form of the BPSK modulation equation is as follows:

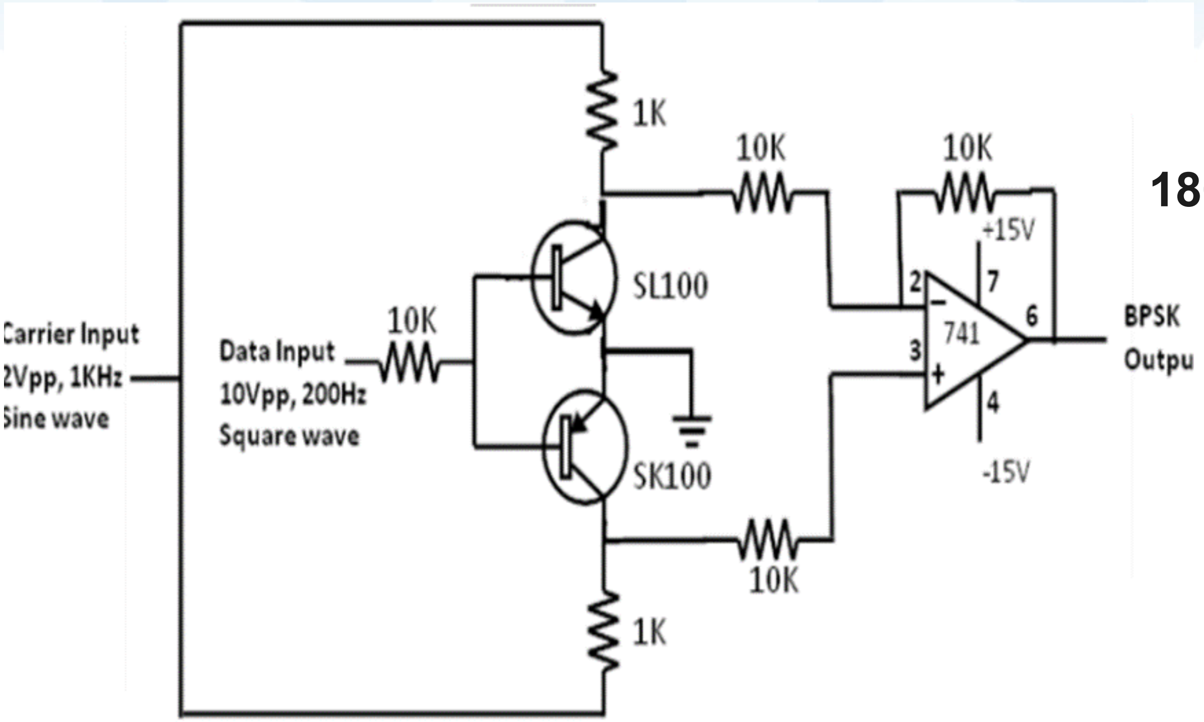
E_b– Energy per bit, T_b – Bit duration

$$C_n(t) = \sqrt{\frac{2E_b}{T_b}} cos\big(2\pi f_c t + \pi(1-n)\big), n = 0, 1.$$

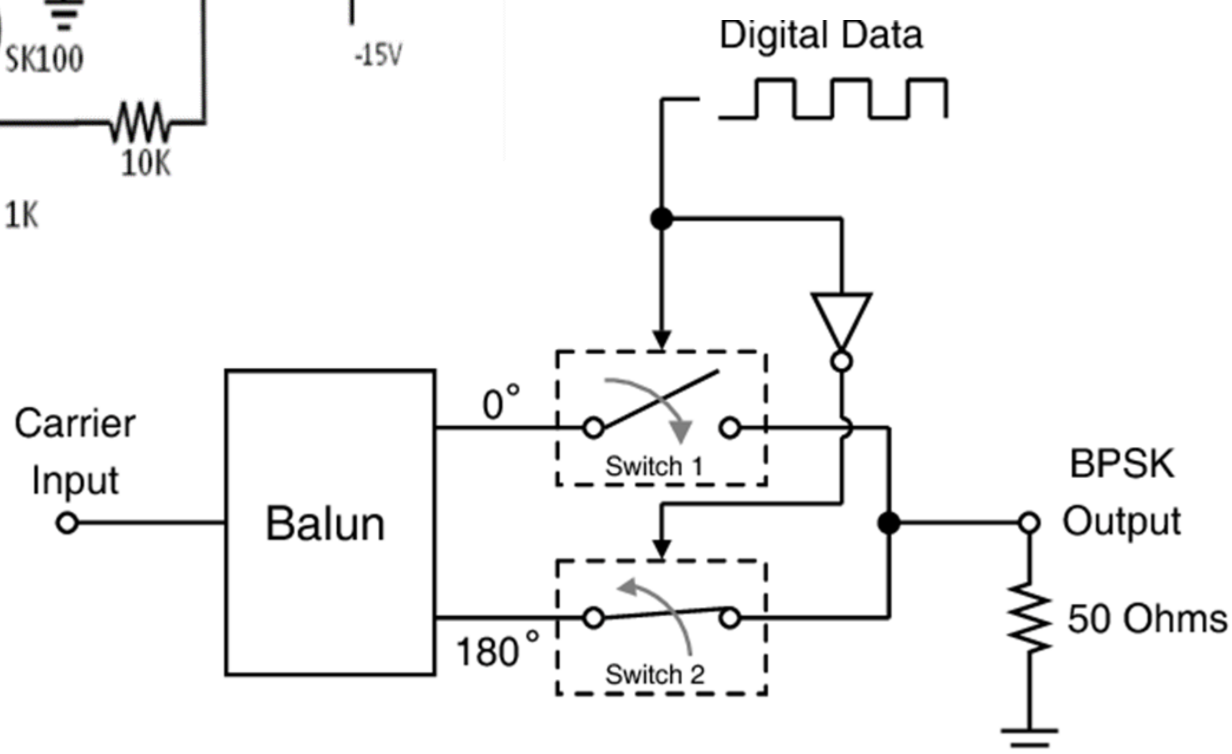
For binary 0, $C_0(t) = -\sqrt{\frac{2E_b}{T_b}} cos(2\pi f_c t)$

For binary 1, $C_1(t) = \sqrt{\frac{2E_b}{T_b}} cos(2\pi f_c t)$

Basic PBSK – Modulator Circuit



180^0 Phase shift



FSK Demodulation

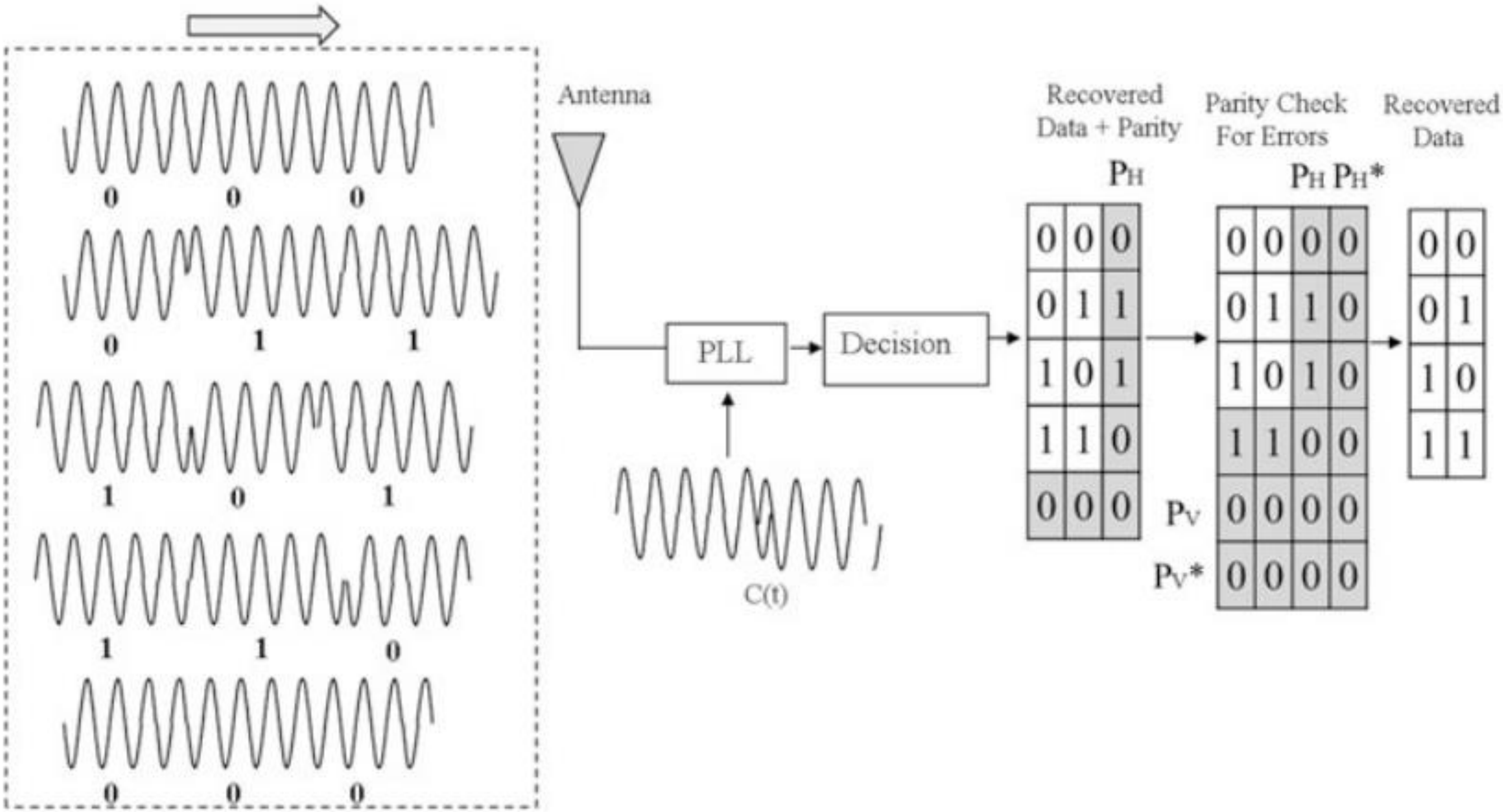
- This is often accomplished with the use of a phase detector, typically known as a phase-locked loop (PLL).

- As the signal enters the receiver, it passes through the PLL. The PLL locks the incoming carrier frequency and tracks the variations in frequency and phase. This is known as the coherent detection technique, where the knowledge of the carrier frequency and phase must be known to the receiver.

- The Following Figure shows a simplified block diagram of a BPSK demodulator along with the data recovery process.

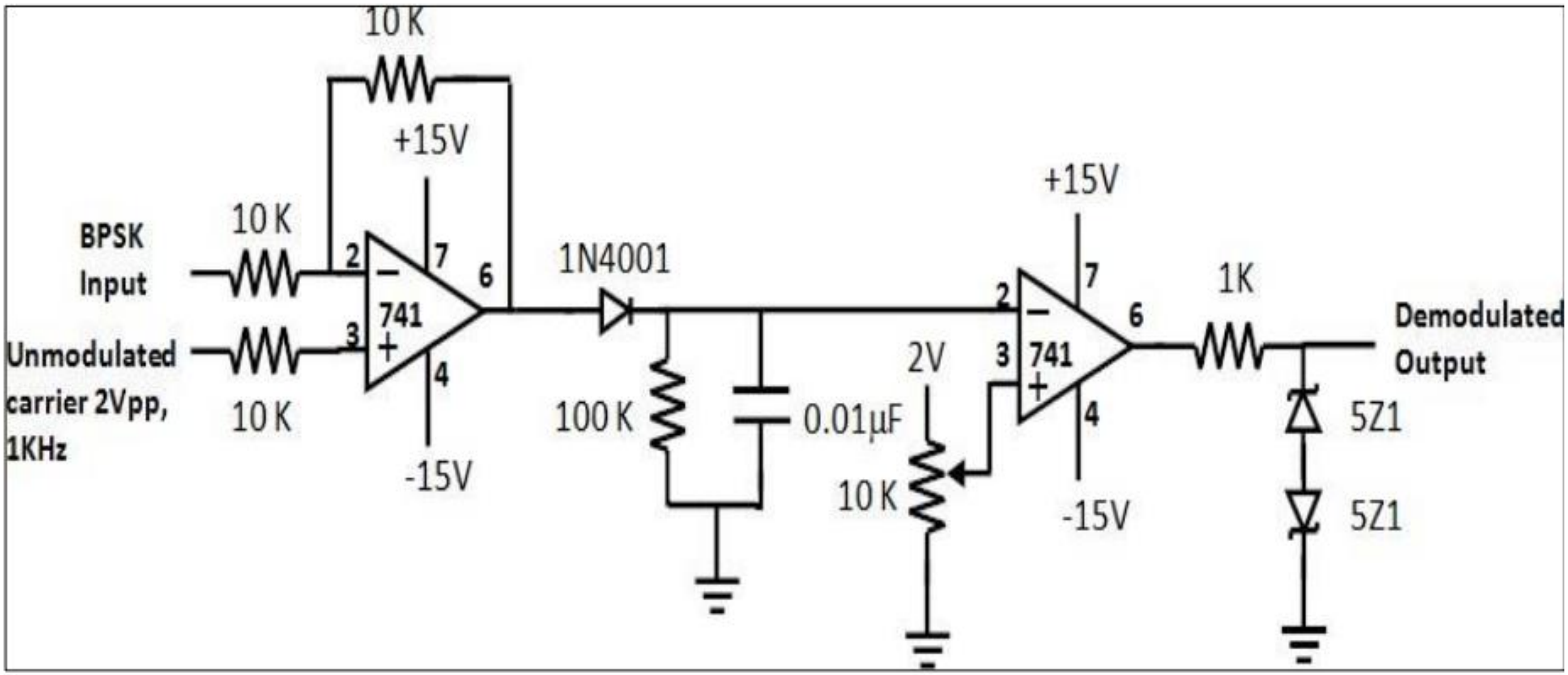
- To ensure that the bits are decoded correctly, the phase deviation needs to be chosen with the limitations of the PLL in mind to eliminate crossover.

BPSK Demodulation



BPSK Demodulation

Basic Demodulation Circuit



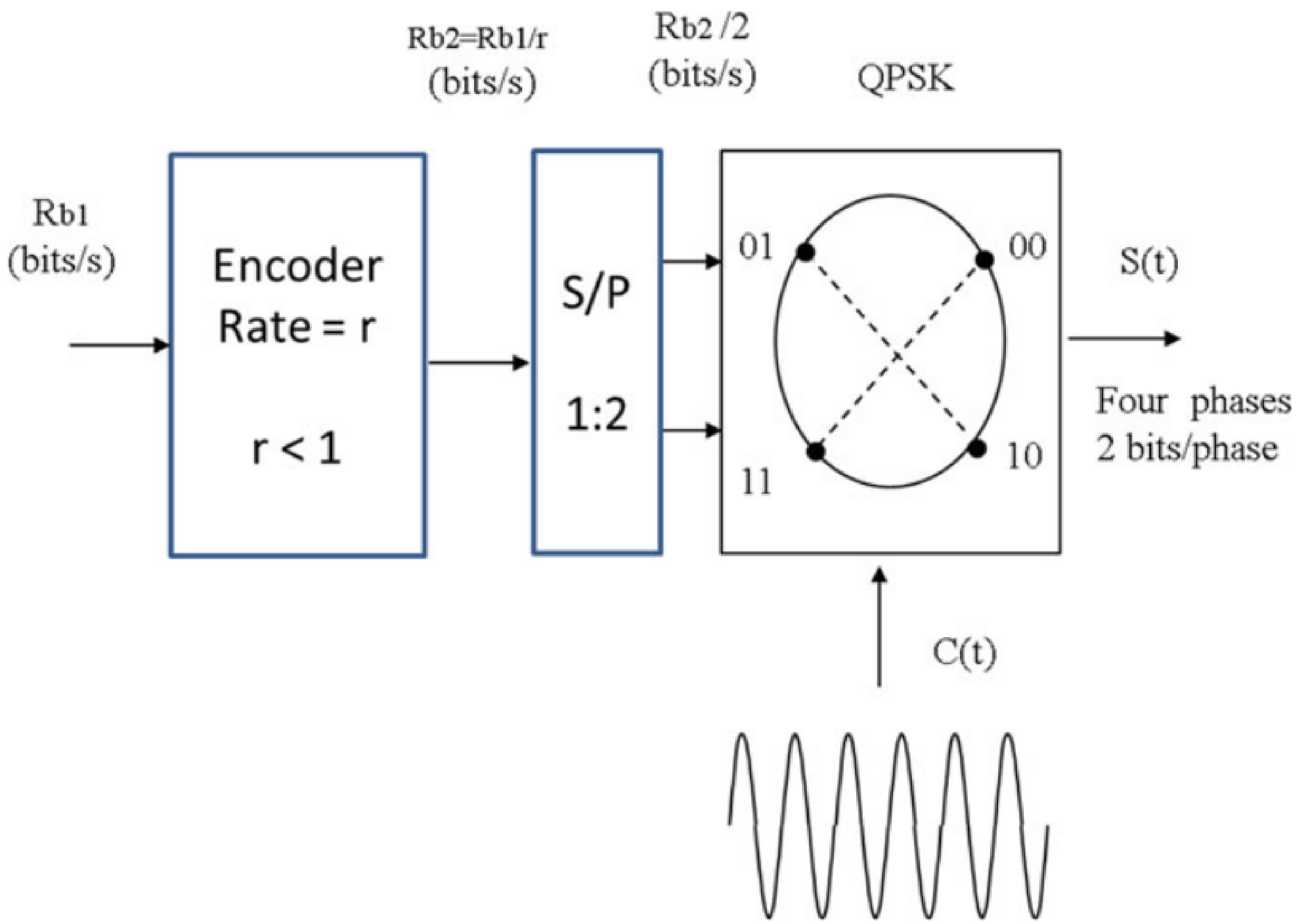
QPSK Modulation

QPSK Modulation

- The input raw data, having a bit rate R_{b1}, is encoded by a rate r (r < 1) encoder. The encoded data, having a bit rate $R_{b2} = R_{b1} /r$, is serial to parallel converted into two parallel streams.
- The encoded bit rate, now reduced in speed by a factor of two, is modulated by the QPSK modulator as shown in the following figure.
- The QPSK modulator takes one bit from each stream to construct the four-phase constellation, also known as "Symbols," where each symbol represents two bits.
- Therefore, the symbol rate is reduced by a factor of two.
- The QPSK modulator has four phases or 4 symbols, 2-bits/symbol as shown in the figure.
- Therefore, the QPSK modulator has the following specifications:
    - 4phases or 4 symbols
    - 2-bits/symbol

QPSK Modulation

QPSK signal constellation having 4 symbols, 2 bits per symbol

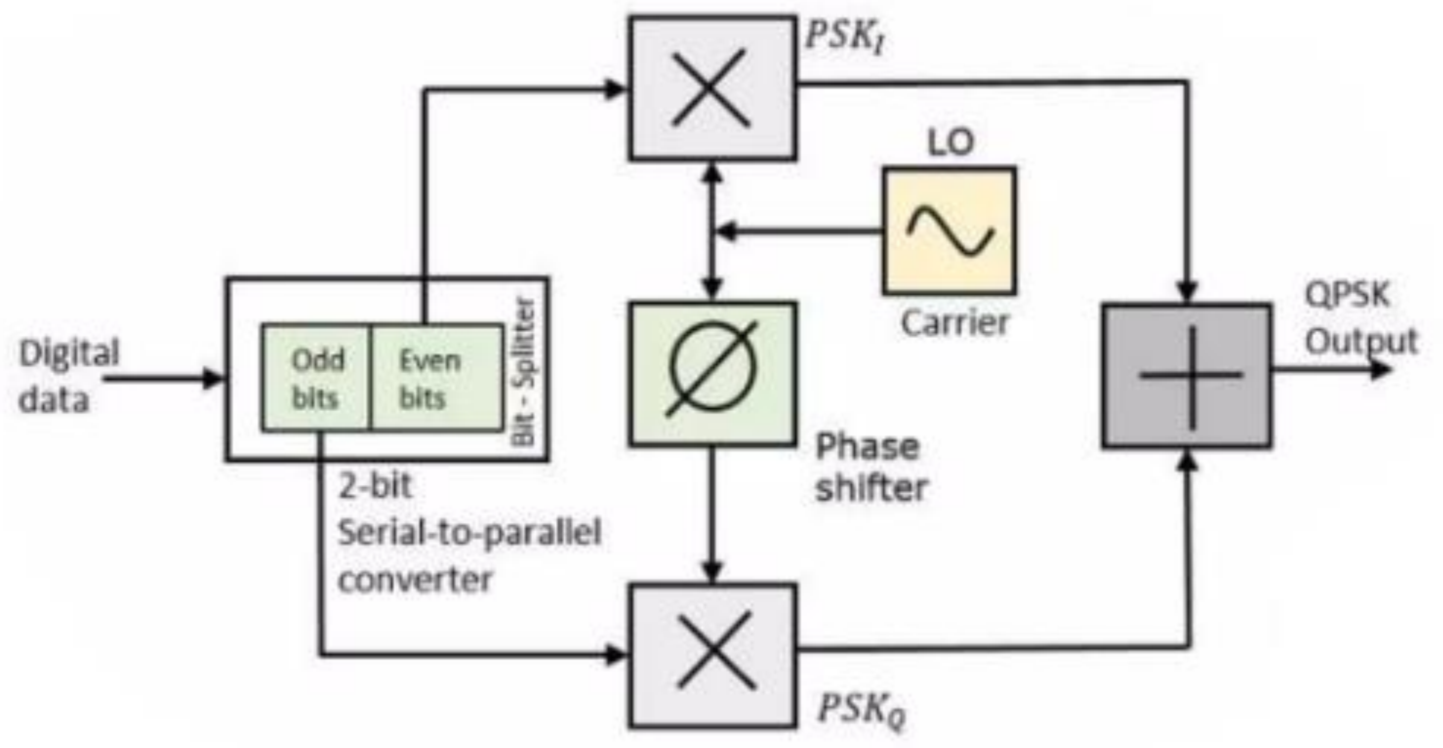


QPSK Modulation

- This is the phase shift keying technique, in which the sine wave carrier takes four phase reversals such as 0°, 90°, 180°, and 270°.
- Instead of the conversion of digital bits into a series of digital stream, it converts them into bit pairs.
- This decreases the data bit rate to half, which allows space for the other users.
- The QPSK Modulator uses a bit splitter, two multipliers with a local oscillator, a 2-bit serial to parallel converter, and a summer circuit.

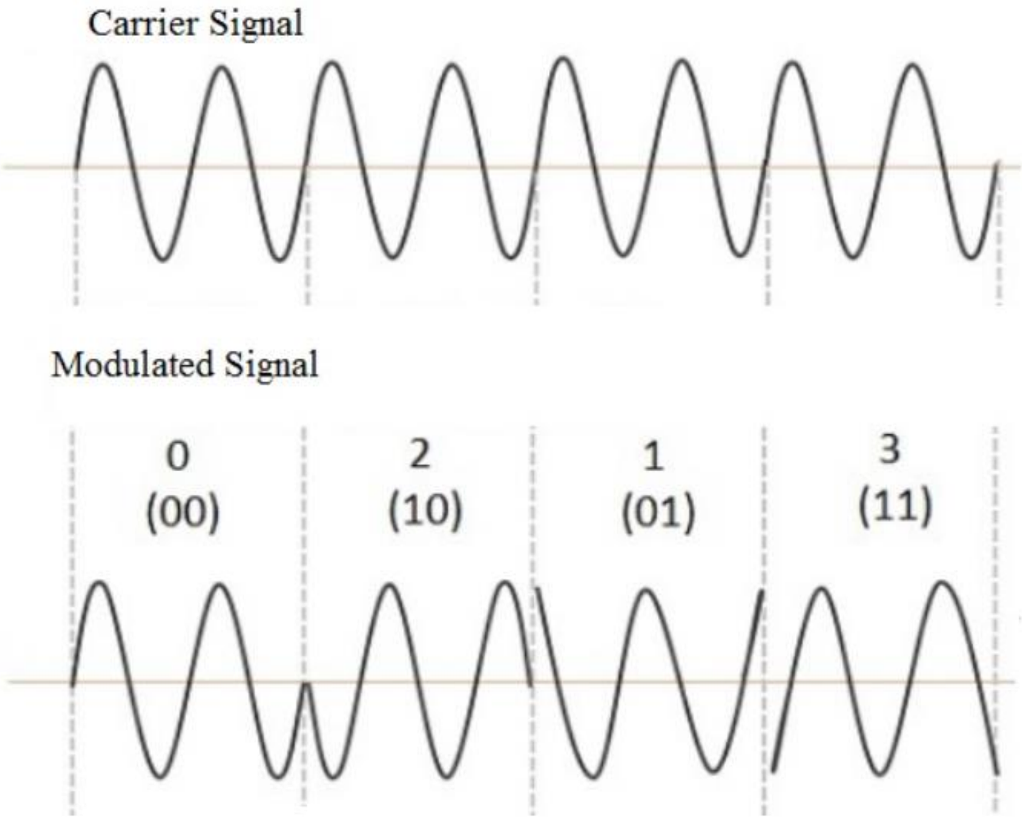
QPSK Modulation

- At the modulator's input, the information signal even bits (2nd, 4th, 6th bit, etc) and odd bits (1st, 3rd, 5th bit, etc) are separated by the bit splitter and multiplied with the same carrier to generate odd BPSK (**PSK_I**) and even BPSK (**PSK_Q**). The PSK_Q signal is phase-shifted by **90^0** before being modulated.



QPSK Modulation

- The QPSK modulated signal for four 2-bit inputs is as follows, which shows the modulated result for different instances of binary inputs.



QPSK Modulation

The QPSK waveform

- With quadrature phase shift keying modulation (QPSK, quadriphase PSK, or 4-PSK), a sinusoidal waveform is varied in phase while keeping the amplitude and frequency constant.
- The term quadrature indicates that there are four possible phases. The following equation shows the general expression for a QPSK waveform.

$$S_i = \mathrm{A}\sin[\omega_c t + \varphi_0 + \varphi_i(t)]$$

S_i - PSK signal waveform for phase i
t – Time
A - Peak Amplitude
ω_c - Carrier frequency
φ_0 - Reference phase angle
φ_i - phase i
i - Range from 1 to 4

➢ **The instantaneous phase has discrete values equal to $\boldsymbol{\varphi_0 + \frac{2\pi i}{4}}$**
i = 1, 2, 3, or 4

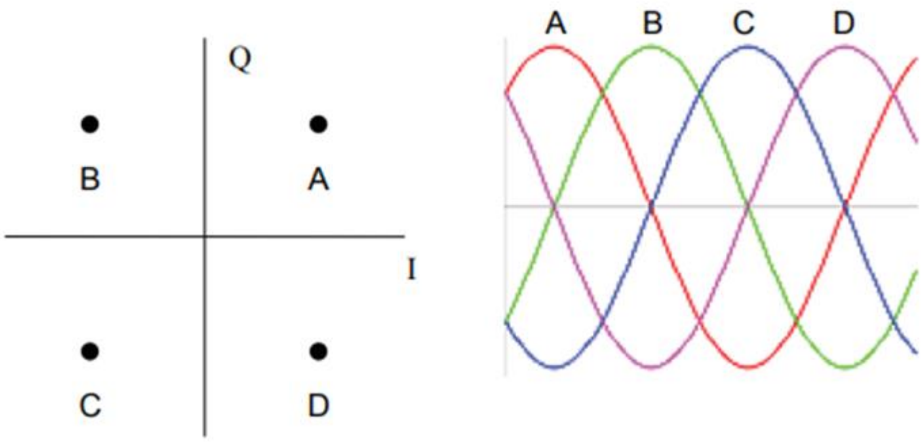
QPSK Modulation

The QPSK constellations

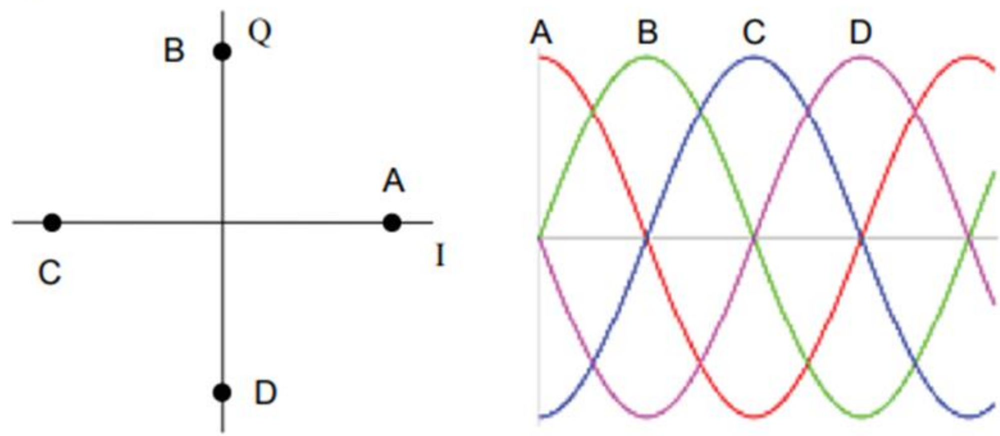
- The ideal PSK constellation has M equidistant phase states and constant amplitude, resulting in circular symmetry. With QPSK, therefore, M = 4, and the phases are separated by 90^0.
- Figure shows two common representations of the QPSK constellation. The constellation points are arbitrarily labeled A, B, C and D, each of which represents one of the four possible dibits 00, 01, 10, and 11.
- The mapping between the dibits and the constellation points depends on the modulator circuit. Beside each constellation in Figure is a plot showing all four phases (modulation symbols) as sinusoids.
- In each of these representations, the four phases are spaced 90^0 ($\pi/2$ radians) apart. The only difference between these representations is the choice of the reference phase angle (φ_0 in the above Equation).

QPSK Modulation

The QPSK constellations



a) QPSK ($\varphi = \pi/4, 3\pi/4, 5\pi/4, 7\pi/4$)



b) QPSK ($\varphi = 0, \pi/2, \pi, 3\pi/2$)

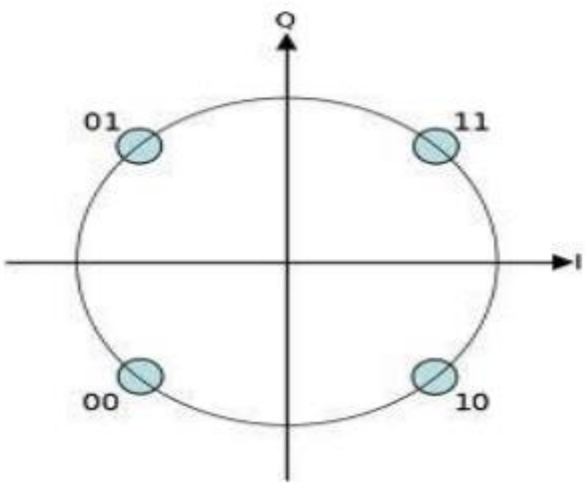
QPSK Modulation

The QPSK constellations

- A QPSK modulator is a double (base 2) signal, to deliver four unique input mixes, 00, 01, 10, and 11 as bellow figure.
- Hence, with QPSK, the twofold information is consolidated into gatherings of two bits, called charges. In the modulator, each charge code produces one of the four conceivable yield phases,)45°,135°,-45°,and - 135°).

$$C_n(t) = \sqrt{\frac{2E_b}{T_b}} cos\left(2\pi f_c t + (2n-1)\frac{\pi}{4}\right), n = 0, 1, 2, 3$$

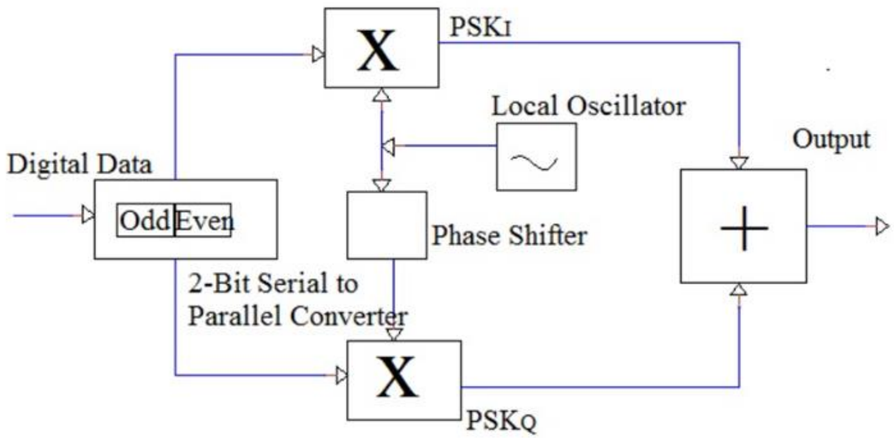
$$\text{QPSK} \quad s(t) = \begin{cases} A\cos\left(2\pi f_c t + \frac{\pi}{4}\right) & 11 \\ A\cos\left(2\pi f_c t + \frac{3\pi}{4}\right) & 01 \\ A\cos\left(2\pi f_c t - \frac{3\pi}{4}\right) & 00 \\ A\cos\left(2\pi f_c t - \frac{\pi}{4}\right) & 10 \end{cases}$$

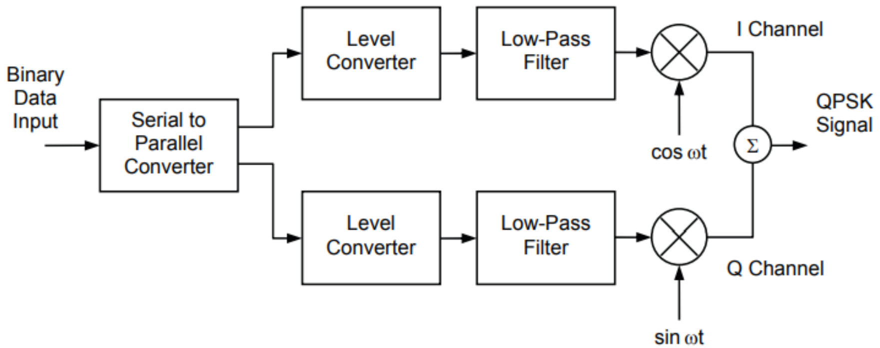


QPSK Modulation

A typical QPSK modulator

- A QPSK signal can be generated by independently modulating two carriers in quadrature (cos(ωt) and sin(ωt)), as shown in below Figure.
- The Serial to Parallel Converter groups the incoming data into dibits (groups of two consecutive bits). Each time two bits have been clocked serially into its buffer, the Serial to Parallel Converter outputs one dibit in parallel at its two outputs.
- One bit of each dibit is sent to the **I channel** of the modulator; the other bit is sent to the **Q channel** of the modulator. Each channel of the modulator works independently to processes the stream of bits it receives.

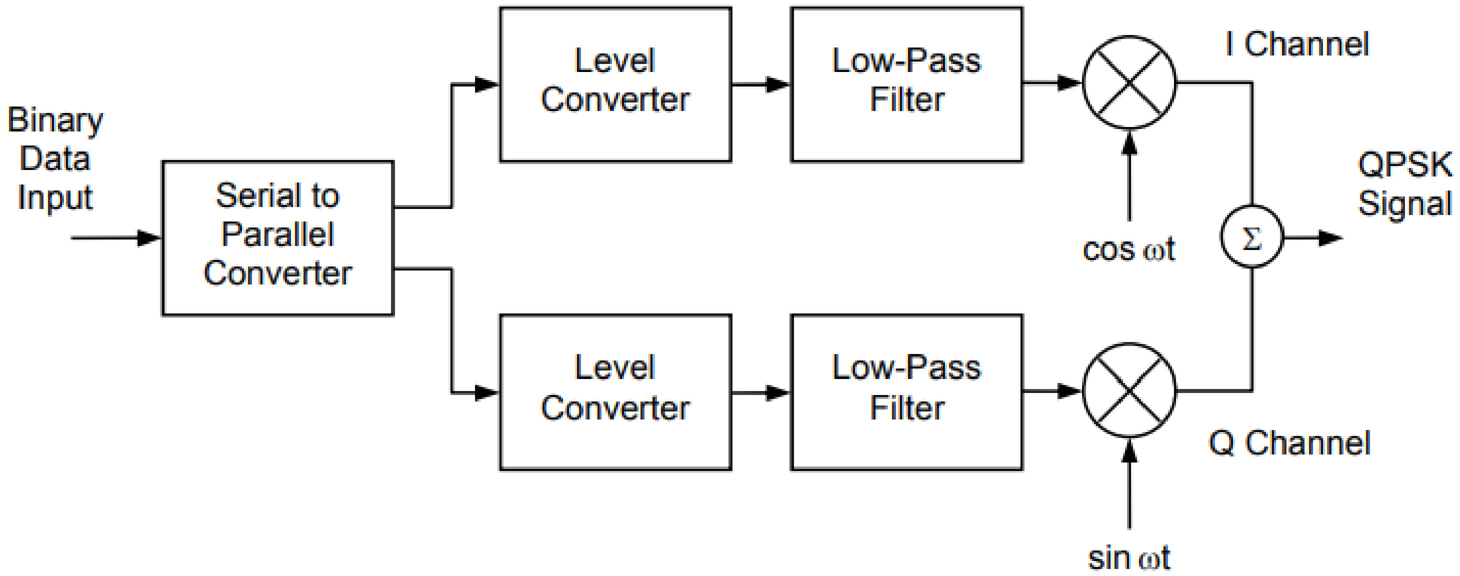




QPSK Modulation

A typical QPSK modulator

- The starting point for grouping bits into dibits is completely arbitrary. For educational purposes, the Serial to Parallel Converter in the QPSK application has a Drop 1 Bit button. Clicking this button causes the Serial to Parallel Converter to ignore one bit in the data sequence. This changes the grouping of all subsequent data bits into dibits.



- The Level Converter in each channel converts the data into a (baseband) bipolar pulse stream that can be applied to one input of the mixer. To restrict the bandwidth of the QPSK signal, a Low-Pass Filter is usually used before the mixer in each channel of the modulator in order to provide the desired spectral shaping.

QPSK Modulation

A typical QPSK modulator

- The I- and Q-channel sinusoidal carriers cos(ωt) and sin(ωt) are in quadrature (90^0 out of phase). Each mixer performs modulation by multiplying the carrier by the bipolar data signal to produce a BPSK signal. The effect of the mixer is to shift the frequency spectrum of the baseband signal up to the frequency of the carrier.
- The two BPSK signals are summed to produce the QPSK signal. Because these two BPSK signals are generated using two carriers in phase quadrature, the BPSK signals are orthogonal, and the QPSK demodulator will be able to demodulate them separately.
- The output signal of the modulator is a sinusoidal carrier with four possible phases, each of which represents a two-bit symbol. This signal can be represented by the following equation.

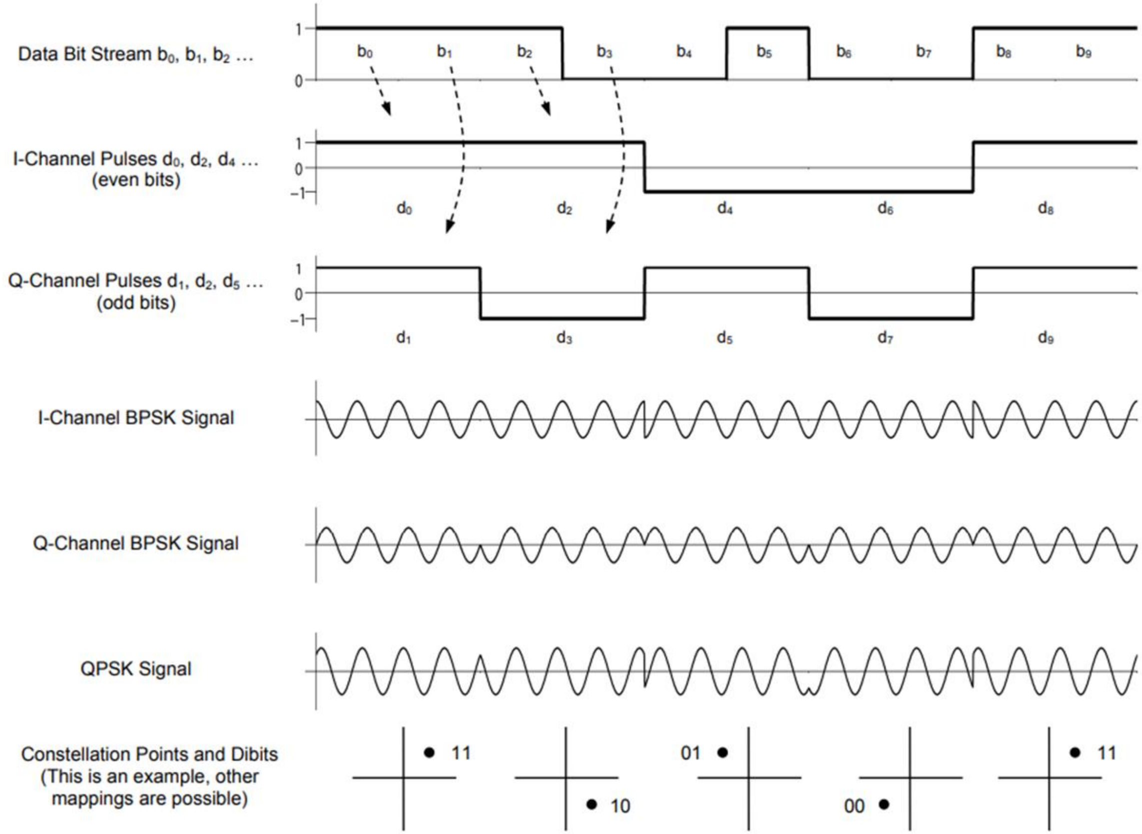
$$S(t) = d_I(\mathrm{t})\, cos(\omega t) + d_Q(t)\, \sin(\omega t)$$

S(t) - QPSK signal waveform
$D_I(t)$ – I channel bipolar pulse stream d_0, d_2, d_4, …
$D_Q(t)$ – Q channel bipolar pulse stream d_1, d_3, d_5, …
ω - Angular frequency

QPSK Modulation

QPSK signal generation from two BPSK signals

- Signal diagram shows the dibit 11 mapped to the constellation point in the first quadrant. Other mappings are possible. Such mappings usually use a Gray code to ensure that only one-bit changes between adjacent symbols. As a result, QPSK modulators map the dibits 00 and 11 to opposite quadrants.



Gray Code – Binary Number Representation

Number Representation

- ***Difficult to represent Decimal numbers directly in a digital system***
- ***Easier to convert them to binary***
- ***Both Decimal and Binary numbers use a positional weighting system***

ex: $1010_2 = 1x2^3+0x2^2+1x2^1+0x2^0 = 1x8 + 0x4 + 1x2 + 0x1 = 10_{10}$

In logic systems different codes in general use

Ex: ***Binary code***
Sign – Binary
One's complement
Two's complement
Hexa Decimal
Binary Code Decimal (BCD)
Grey Code
ASCII Code

- ***Representing negative numbers***
  (Sign – Binary, One's complement, Two's complement)

Gray Code

- *It is not a weighted and arithmetic code*
- *The grey code exhibits only a single bit change from one code word to the next in sequence*
- *It has no intermediate state in transition from one position to another*

4 Bit grey code

DECIMAL	BINARY	GRAY CODE	DECIMAL	BINARY	GRAY CODE
0	0000	0000	8	1000	1100
1	0001	0001	9	1001	1101
2	0010	0011	10	1010	1111
3	0011	0010	11	1011	1110
4	0100	0110	12	1100	1010
5	0101	0111	13	1101	1011
6	0110	0101	14	1110	1001
7	0111	0100	15	1111	1000

American Standard Code for Information Interchange (ASCII)

- *It is Universally accepted alphanumeric code used in most computer and other electronic devices*
- *Has 128 characters and symbols represented by a 7 bit binary code*
- *First 32 control characters are represented by 00 to 1F Hexadecimal*
- *The graphic symbols are listed from 20h to 7Fh*
- *The extended ASCII characters are represented by an 8-bit code series from 80h to FFh*

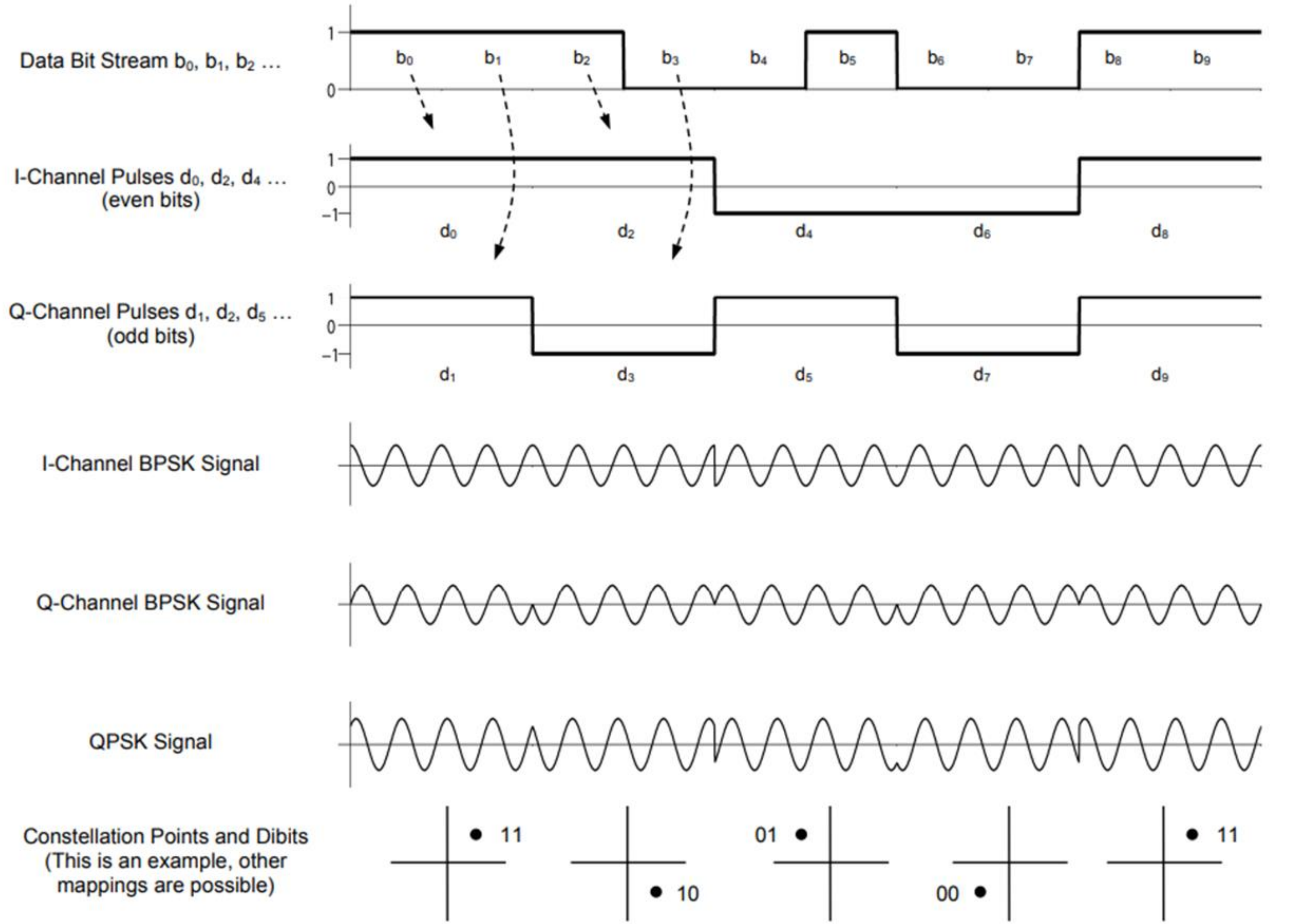
ASCII Control Characters

NAME	DECIMAL	HEX	KEY	DESCRIPTION
NUL	0	00	CTRL @	null character
SOH	1	01	CTRL A	start of header
STX	2	02	CTRL B	start of text
ETX	3	03	CTRL C	end of text
EOT	4	04	CTRL D	end of transmission
ENQ	5	05	CTRL E	enquire
ACK	6	06	CTRL F	acknowledge
BEL	7	07	CTRL G	bell
BS	8	08	CTRL H	backspace
HT	9	09	CTRL I	horizontal tab
LF	10	0A	CTRL J	line feed
VT	11	0B	CTRL K	vertical tab
FF	12	0C	CTRL L	form feed (new page)
CR	13	0D	CTRL M	carriage return
SO	14	0E	CTRL N	shift out
SI	15	0F	CTRL O	shift in
DLE	16	10	CTRL P	data link escape
DC1	17	11	CTRL Q	device control 1
DC2	18	12	CTRL R	device control 2
DC3	19	13	CTRL S	device control 3
DC4	20	14	CTRL T	device control 4
NAK	21	15	CTRL U	negative acknowledge
SYN	22	16	CTRL V	synchronize
ETB	23	17	CTRL W	end of transmission block
CAN	24	18	CTRL X	cancel
EM	25	19	CTRL Y	end of medium
SUB	26	1A	CTRL Z	substitute
ESC	27	1B	CTRL [	escape
FS	28	1C	CTRL /	file separator
GS	29	1D	CTRL]	group separator
RS	30	1E	CTRL ^	record separator
US	31	1F	CTRL _	unit separator

SYMBOL	DEC	HEX	SYMBOL	DEC	HEX	SYMBOL	DEC	HEX	SYMBOL	DEC	HEX
Ç	128	80	á	160	A0	└	192	C0	α	224	E0
ü	129	81	í	161	A1	┴	193	C1	β	225	E1
é	130	82	ó	162	A2	┬	194	C2	Γ	226	E2
â	131	83	ú	163	A3	├	195	C3	π	227	E3
ä	132	84	ñ	164	A4	─	196	C4	Σ	228	E4
à	133	85	Ñ	165	A5	┼	197	C5	σ	229	E5
å	134	86	ª	166	A6	╞	198	C6	µ	230	E6
ç	135	87	º	167	A7	╟	199	C7	τ	231	E7
ê	136	88	¿	168	A8	╚	200	C8	Φ	232	E8
ë	137	89	⌐	169	A9	╔	201	C9	Θ	233	E9
è	138	8A	¬	170	AA	╩	202	CA	Ω	234	EA
ï	139	8B	½	171	AB	╦	203	CB	δ	235	EB
î	140	8C	¼	172	AC	╠	204	CC	∞	236	EC
ì	141	8D	¡	173	AD	═	205	CD	φ	237	ED
Ä	142	8E	«	174	AE	╬	206	CE	ε	238	EE
Å	143	8F	»	175	AF	╧	207	CF	∩	239	EF
É	144	90	░	176	B0	╨	208	D0	≡	240	F0
æ	145	91	▒	177	B1	╤	209	D1	±	241	F1
Æ	146	92	▓	178	B2	╥	210	D2	≥	242	F2
ô	147	93	│	179	B3	╙	211	D3	≤	243	F3
ö	148	94	┤	180	B4	╘	212	D4	⌠	244	F4
ò	149	95	╡	181	B5	╒	213	D5	⌡	245	F5
û	150	96	╢	182	B6	╓	214	D6	÷	246	F6
ù	151	97	╖	183	B7	╫	215	D7	≈	247	F7
ÿ	152	98	╕	184	B8	╪	216	D8	°	248	F8
Ö	153	99	╣	185	B9	┘	217	D9	•	249	F9
Ü	154	9A	║	186	BA	┌	218	DA	·	250	FA
¢	155	9B	╗	187	BB	█	219	DB	√	251	FB
£	156	9C	╝	188	BC	▄	220	DC	η	252	FC
¥	157	9D	╜	189	BD	▌	221	DD	²	253	FD
Pt	158	9E	╛	190	BE	▐	222	DE	■	254	FE
ƒ	159	9F	┐	191	BF	▀	223	DF	□	255	FF

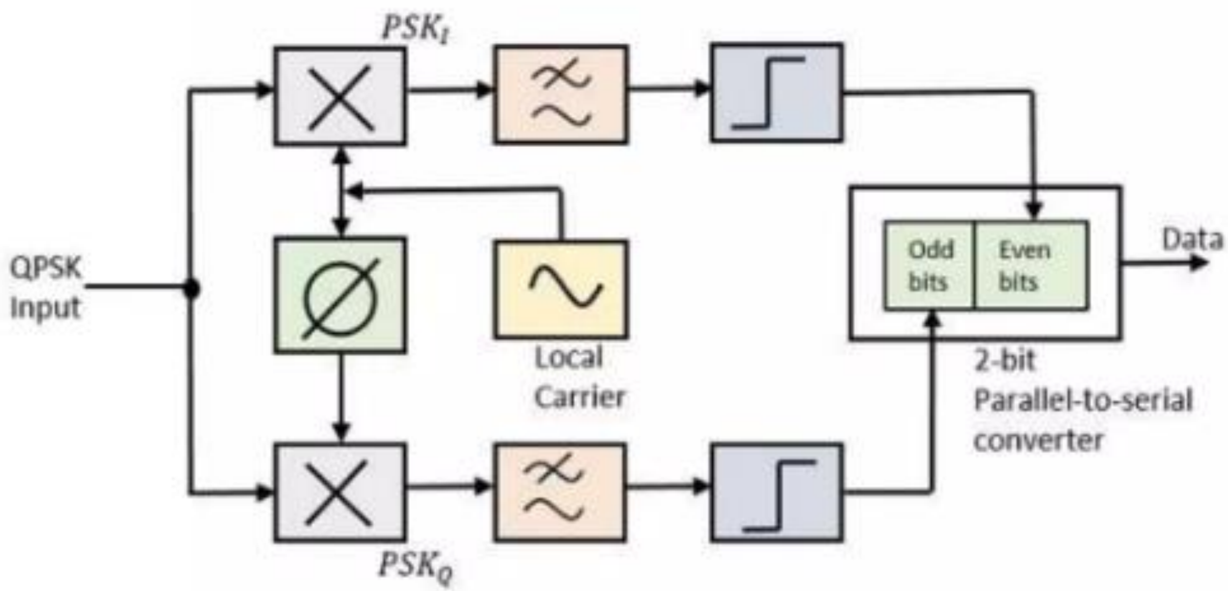
Extended ASCII Characters

QPSK signal generation from two BPSK signals



QPSK Demodulation

- The QPSK Demodulator uses two product demodulator circuits with local oscillator, two band pass filters, two integrator circuits, and a 2-bit parallel to serial converter. Following is the diagram for the same.
- The two product detectors at the input of the demodulator simultaneously demodulate the two BPSK signals.
- The pair of bits are recovered here from the original data. These signals after processing, are passed to the parallel to serial converter.

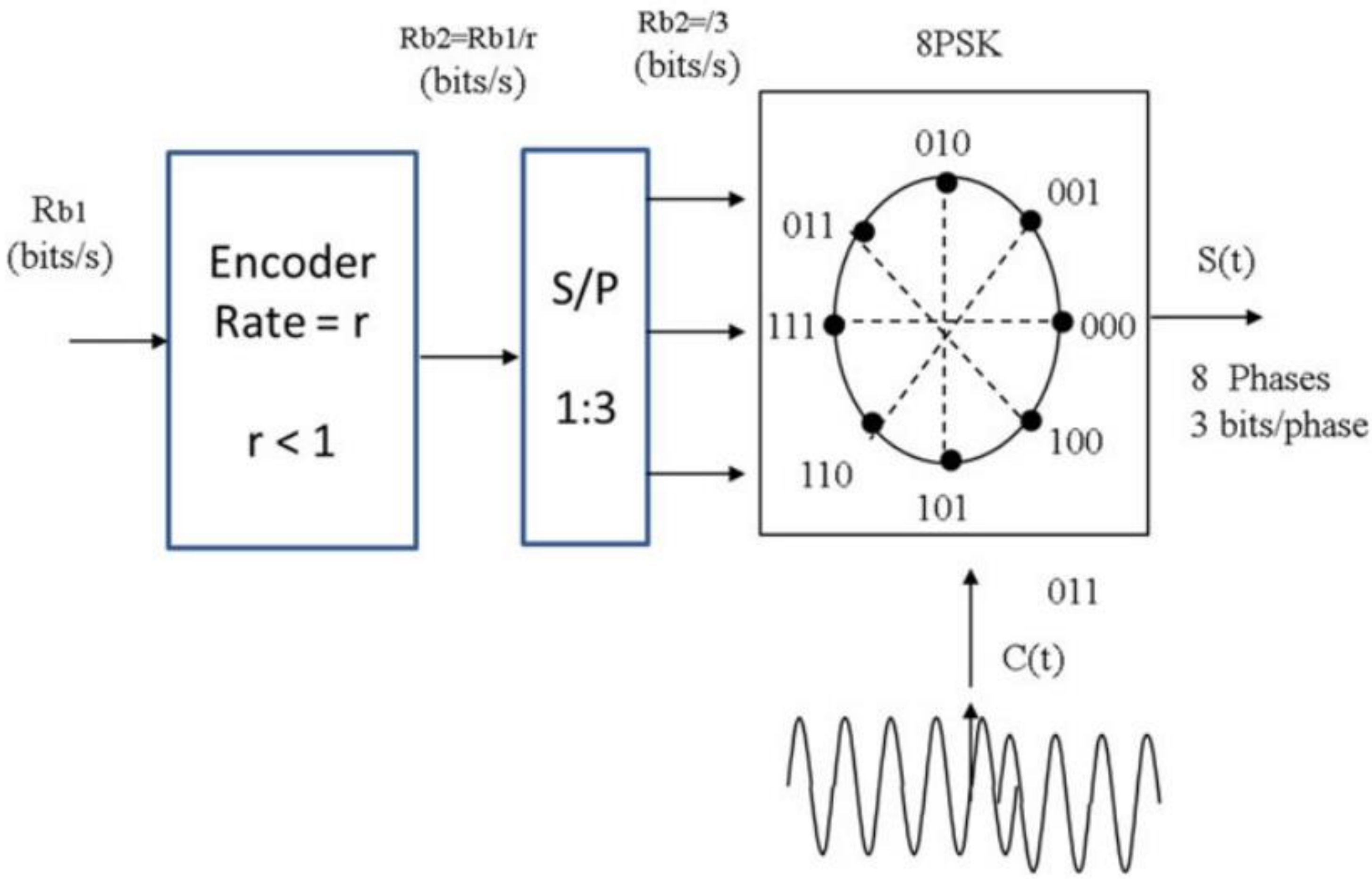


8PSK Modulation

- In 8PSK, the input raw data, having a bit rate R_{b1}, is encoded by a rate r (r < 1) encoder. The encoded data, having a bit rate $R_{b2} = R_{b1}/r$, is serial to parallel converted into three parallel streams.
- The encoded bit rate, now reduced in speed by a factor of three, is modulated by the 8PSK modulator as shown in bellow figure.
- The 8PSK modulator takes one bit from each stream to construct the phase constellation having 8 phases, also known as “Symbols,” where each symbol represents 3-bits.
- The symbol rate is therefore reduced by a factor of 3. The 8PSK modulator has 8 phases or 8 symbols, 3-bits/symbol as shown in the figure.
- Therefore, the 8PSK modulator has the following specifications:
    - 8 phases or 8 symbols
    - 3-bits/symbol

8PSK Modulation

8PSK signal constellation having 8 symbols, 3 bits per symbol

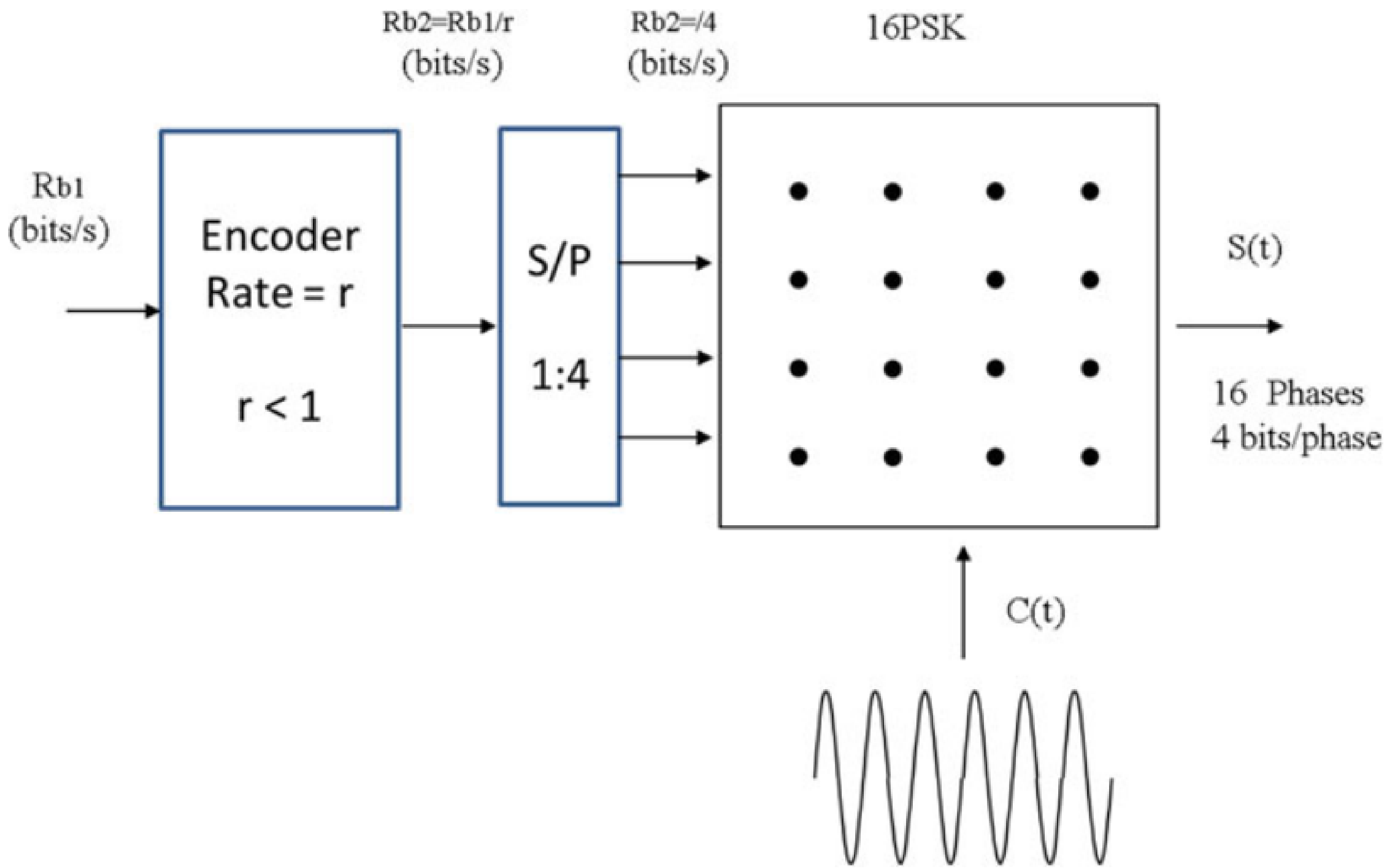


16PSK Modulation

- In 16PSK, the input raw data, having a bit rate R_{b1}, is encoded by means of a rate r (r < 1) encoder. The encoded data, having a bit rate $R_{b2} = R_{b1}/r$, is serial to parallel converted into four parallel streams.
- The encoded bit rate, now reduced in speed by a factor of four, is modulated by the 16PSK modulator as shown in the bellow figure.
- The 16PSK modulator takes one bit from each stream to construct the phase constellation having 16 phases, also known as “Symbols,” where each symbol represents four bits.
- The symbol rate is therefore reduced by a factor of four.
- Therefore, the 16PSK modulator has 16 phases or 16 symbols, 4 bits/symbol as shown in the figure.
- So, the 16PSK modulator has the following specifications: **16 phases or 16 symbols and 4-bits/symbol.**

16PSK Modulation

16PSK signal constellation having 16 symbols, 4-bits per symbol. Here, each symbol is represented by a dot, where each dot represents 4-bits



16PSK Modulation

- **The number of phases and the corresponding bits per phase for MPSK modulation schemes for M = 2, 4, 8, 16, 32, 64, etc…**

Modulation	Number of phases φ	Number of bits per phase
BPSK	2	1
QPSK	4	2
8PSK	8	3
16	16	4
32	32	5
64	64	6
:	:	:

PSK Bandwidth

In digital communications, data is generally referred to as a non-periodic digital signal. It has two values:

- Binary-1 = High, Period = T
- Binary-0 = Low, Period = T

Also, data can be represented in two ways:

- Time domain representation and
- Frequency domain representation

The time domain representation, known as non-return-to-zero (NRZ), is given by:

$$\begin{aligned} V(t) &= V \qquad < 0 < t < T \\ &= 0 \qquad \text{elsewhere} \end{aligned}$$

PSK Bandwidth

The frequency domain representation is given by "Fourier transform"

$$V(\omega) = \int_0^T V \cdot e^{-j\omega t} dt$$

P(ω) - Power spectral density

$$|V(\omega)| = 2\left(\frac{V}{\omega}\right)\sin\left(\frac{\omega T}{2}\right) = VT\left[\frac{\sin(\omega T/2)}{\omega T/2}\right]$$

$$P(\omega) = \left(\frac{1}{T}\right)|V(\omega)|^2 = V^2 T\left[\frac{\sin(\omega T/2)}{\omega T/2}\right]^2$$

- The bandwidth of the power spectrum is proportional to the frequency.
- The one-sided bandwidth is given by the ratio $f/f_b = 1$. So, the one-sided bandwidth = $f = f_b$, where $f_b = R_b = 1/T$, T being the bit duration. The general equation for two-sided response is given by:

$$V(\omega) = \int_{-\infty}^{\infty} V(t) \cdot e^{-j\omega t} dt$$

PSK Bandwidth

- $V(\omega)$ - two-sided spectrum of $V(t)$.
- This is due to both positive and negative frequencies used in the integral.
- The function can be a voltage or a current.

$$V(\omega) = \int_{-\propto}^{\propto} V(t) \cdot e^{-j\omega t} dt$$

Two-sided bandwidth (BW) = $2R_b$ (R_b - Bit rate before coding)

PSK Bandwidth

Fig (a): Discrete-time digital signal

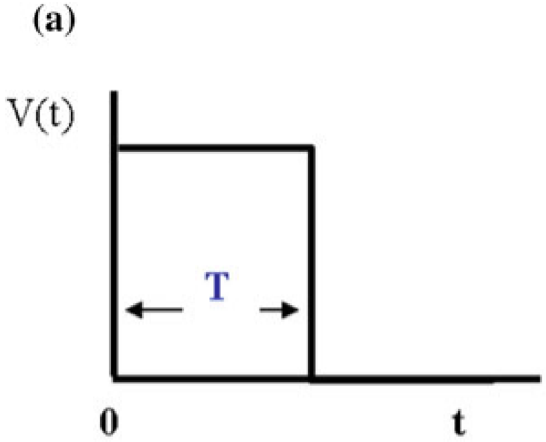


Fig (b): one-sided power spectral density

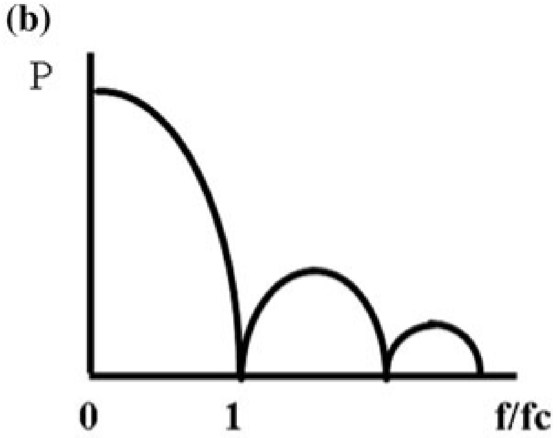
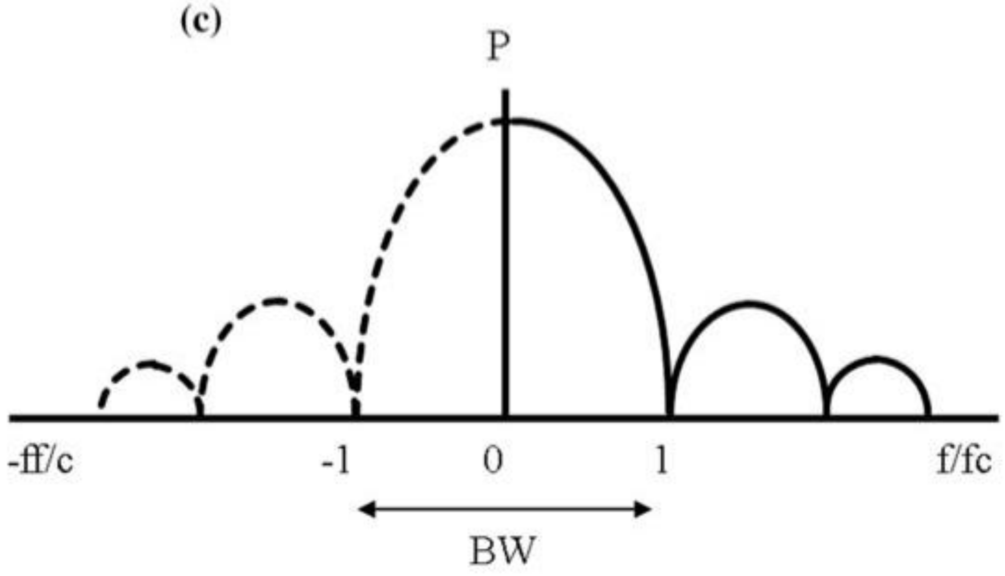


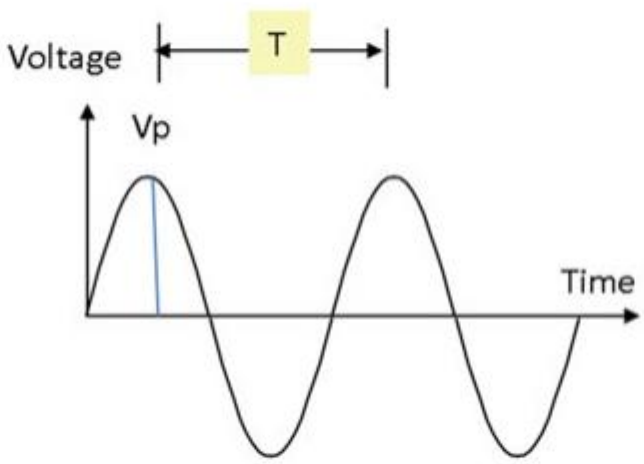
Fig (c): Two-sided power spectral density

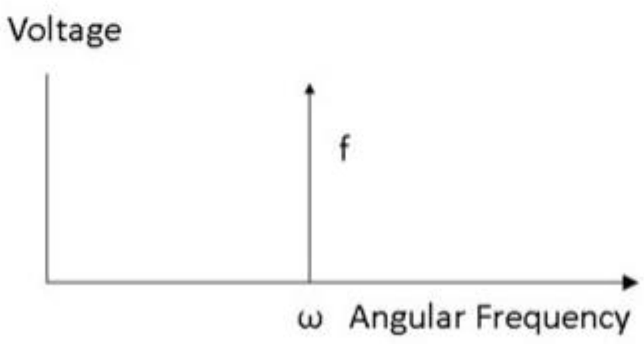


PSK Bandwidth

Spectral Response of the Carrier Before Modulation

$V(t) = V_p \sin(\omega t_c)$ $\quad V_P = \text{Peak voltage}$ $\quad \omega_c = 2\pi f_c$, f_c = Carrier frequency in Hz





PSK Bandwidth

BPSK Spectrum

- The input is a digital signal, and it contains an infinite number of harmonically related sinusoidal waveforms.

$$|V(\omega)| = 2\left(\frac{V}{\omega}\right)\sin\left(\frac{\omega T}{2}\right) = VT\left[\frac{\sin(\omega T/2)}{\omega T/2}\right]$$

- Here, V (ω) is the frequency domain representation of the input digital signal, which has a sin(x)/x response that governs the phase of the carrier frequency. With V(t) = m(t), we write the following as:

$$S(t) = A_c \cos[\omega_c t + \beta\, m(t)]$$

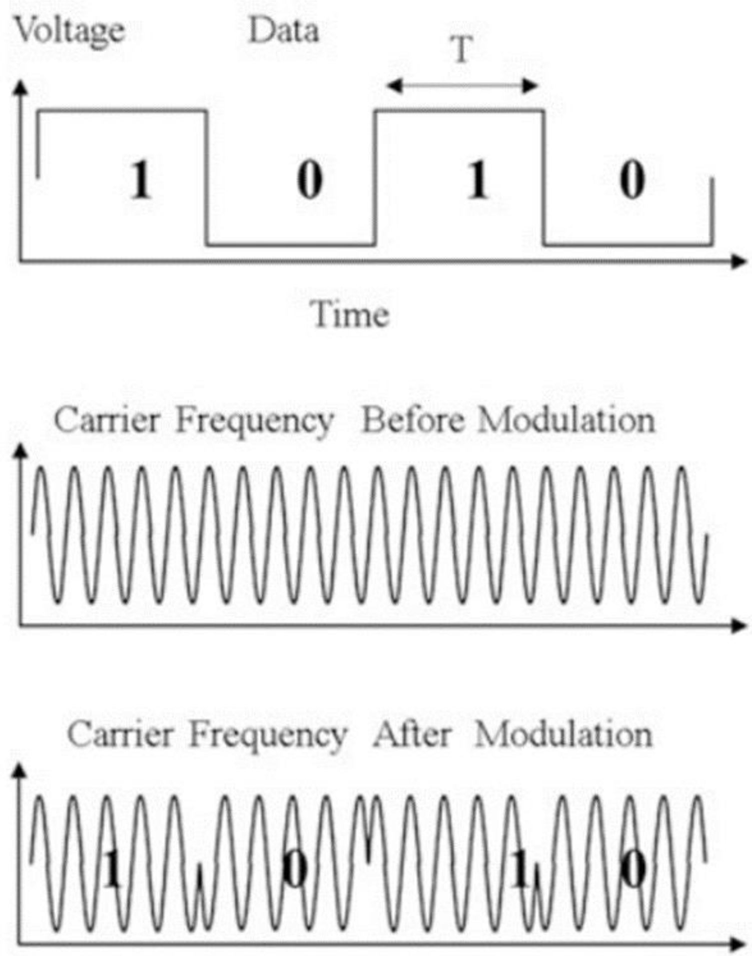
- β is the phase deviation index of the carrier and m(t) has a sin(x)/x response, which is given by

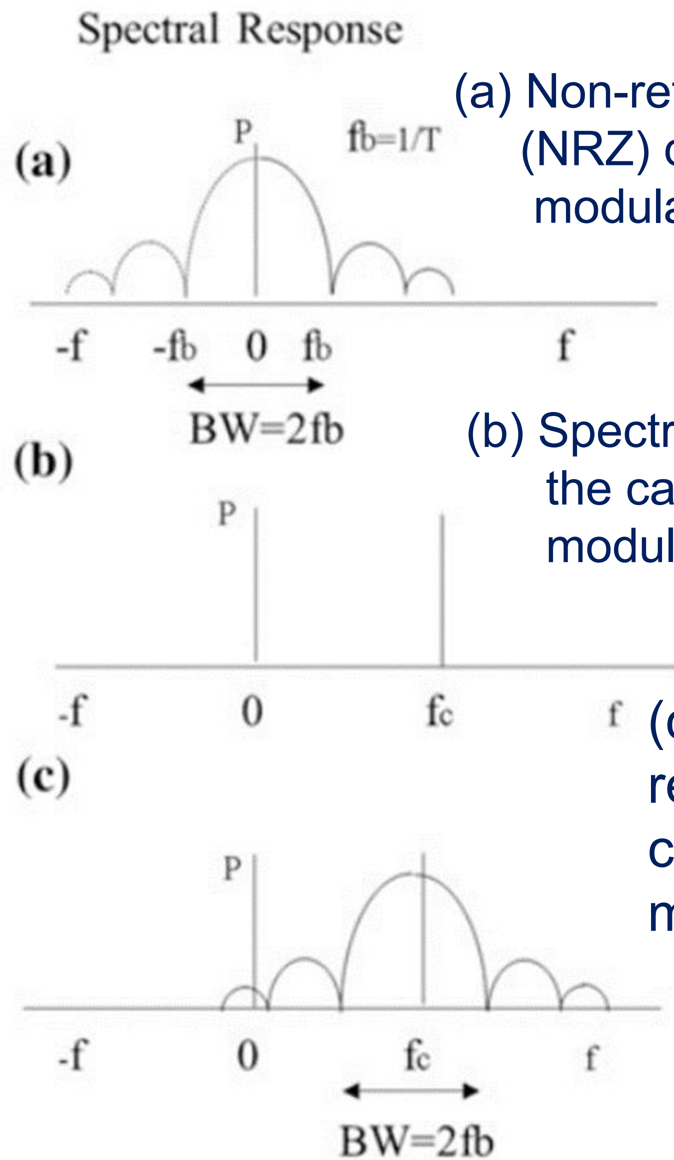
$$m(t) = VT\left[\frac{\sin(\omega m T/2)}{\omega m T/2}\right]$$

- the spectral response after BPSK modulation also has a sin(x)/x response, which is the shifted version of the NRZ data, centered on the carrier frequency fc, as shown in the below figure.

PSK Bandwidth

The spectral response





(a) Non-return-to-zero (NRZ) data before modulation.

(b) Spectral response of the carrier before modulation.

(c) The Spectral response of the carrier after modulation.

BPSK Bandwidth

- R_{b2} - coded bit rate (bit frequency).
- BPSK bandwidth is the same as the ASK bandwidth.

$$\begin{aligned} \text{BW (BPSK)} &\approx 2R_{b2}/\text{Bit per Phase} \\ &\approx 2R_{b2}/1 \approx 2R_{b2} \end{aligned}$$